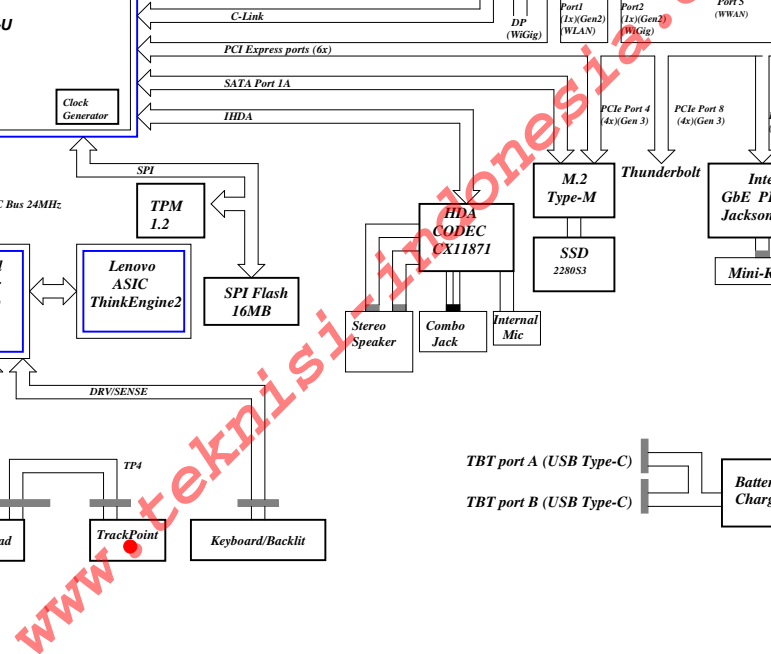


Project Code: 4PD0A9010001 *2016 May ' 05*
PCB(Raw Card): 16822-SA



PCB Layer Stackup		
L1-Component		
L2-GND		
L3-Signal 1		
L4-VCC		
L5-Signal 2		
L6-Signal 3		
L7-VCC		
L8-Signal 4		
L9-GND		
L10-Component		
Battery Charger/Selector		
BQ24780		72/72
VEN270	CHARGER_OUT1	
System DC/DC		
TPS51285		74
VEN270	VCC5M	
CPU DC/DC		
NCP81208/NC1382		75/76
VEN270	VCCCPUCORE	
GMCH GFX CORE		
NCP81382		77
VEN270	VCCGFXCORE	
VCCSA		
NCP81383		78
VEN270	VCCSA	
VCCCPU10		
TPS6D134A		80
VCC5M	VCCCPU10	
VCCIR05US		
BD91364AM		81
VCC5M	VCCIR05_US	
VCCIR2A		
SN1490027		83
VEN270	VCCIR2A	
VCCOR06B		
TPS51206DSQR		84
VCCIR2A	VCCOR06B	
VCCIR8R5US		
BU90004GWZ		85
VCC5M	VCCIR8_US	
VCCPCCHORE		
TPS6D134D		86
VCC5M	VCCPCCHORE	
VCCIR8A		
BU90004GWZ		97
VCC5M	VCCIR8A	

RESISTOR

Symbol name	Value	Tolerance (J: 5%, F: 1%, D: 0.5%, B: 0.1 %)	Rating 0402=> 1/16W, 25V 0603 => 1/16W, 75V 0805 => 1/10W, 100V	Size 2=>0402, 3=>0603, 5=>0805 6=>1206, 0=>1210
10KR3	10K Ohm	If no letter, it means J: 5%	1/16W, 75V	0603
33D3R5	33.3 Ohm	If no letter, it means J: 5%	1/10W, 100V	0805
1KR3F	1K Ohm	F: 1%	1/16W, 75V	0603

The naming rule is value + R + size + tolerance
For the value, it can be read by the number before R. (R means resistor)
For the tolerance, it can be read from the last letter.
For the rating, we don't show on the symbol name.
For the size, R2=>0402, R3=>0603, R5=>0805,....

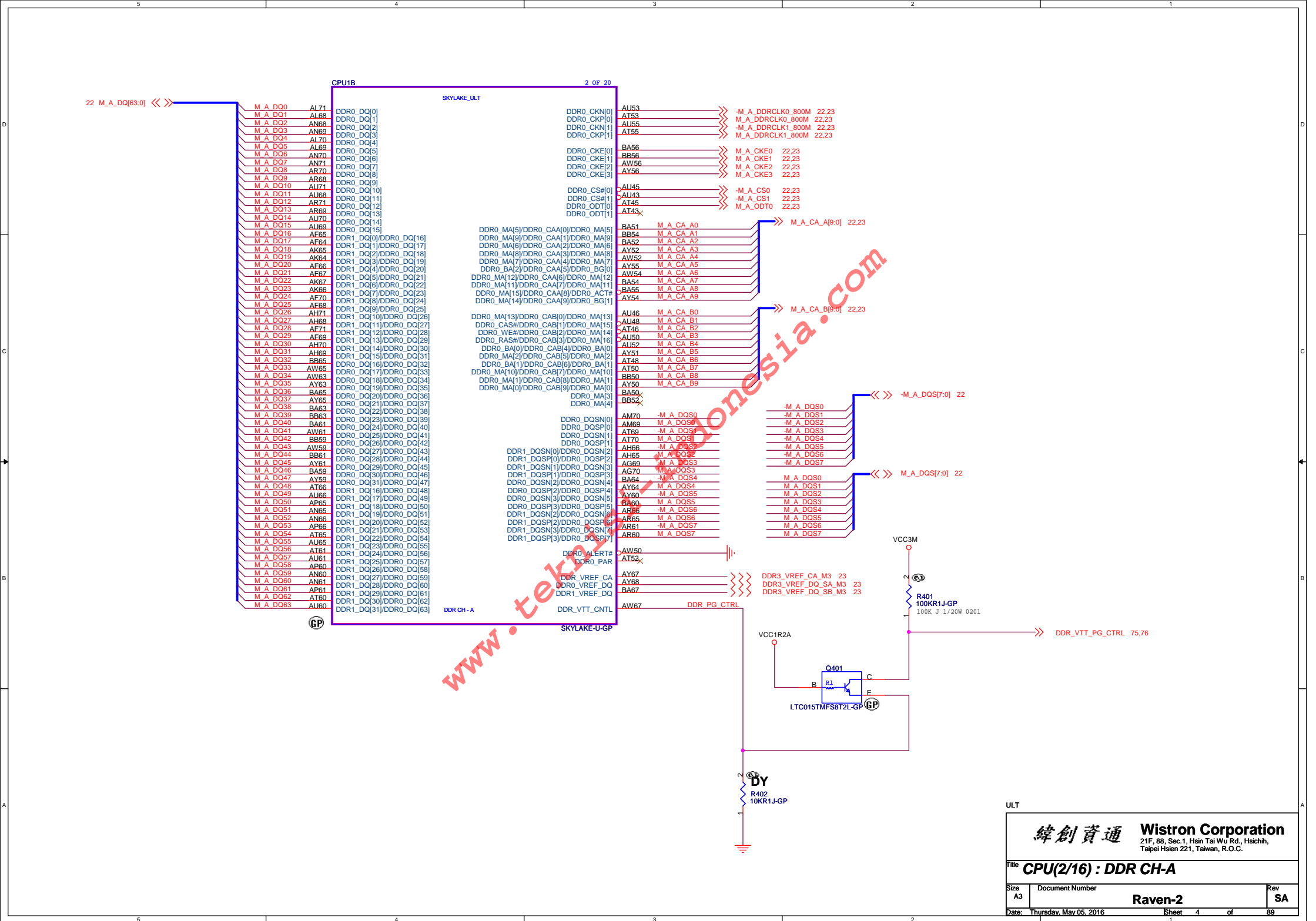
CAPACITOR

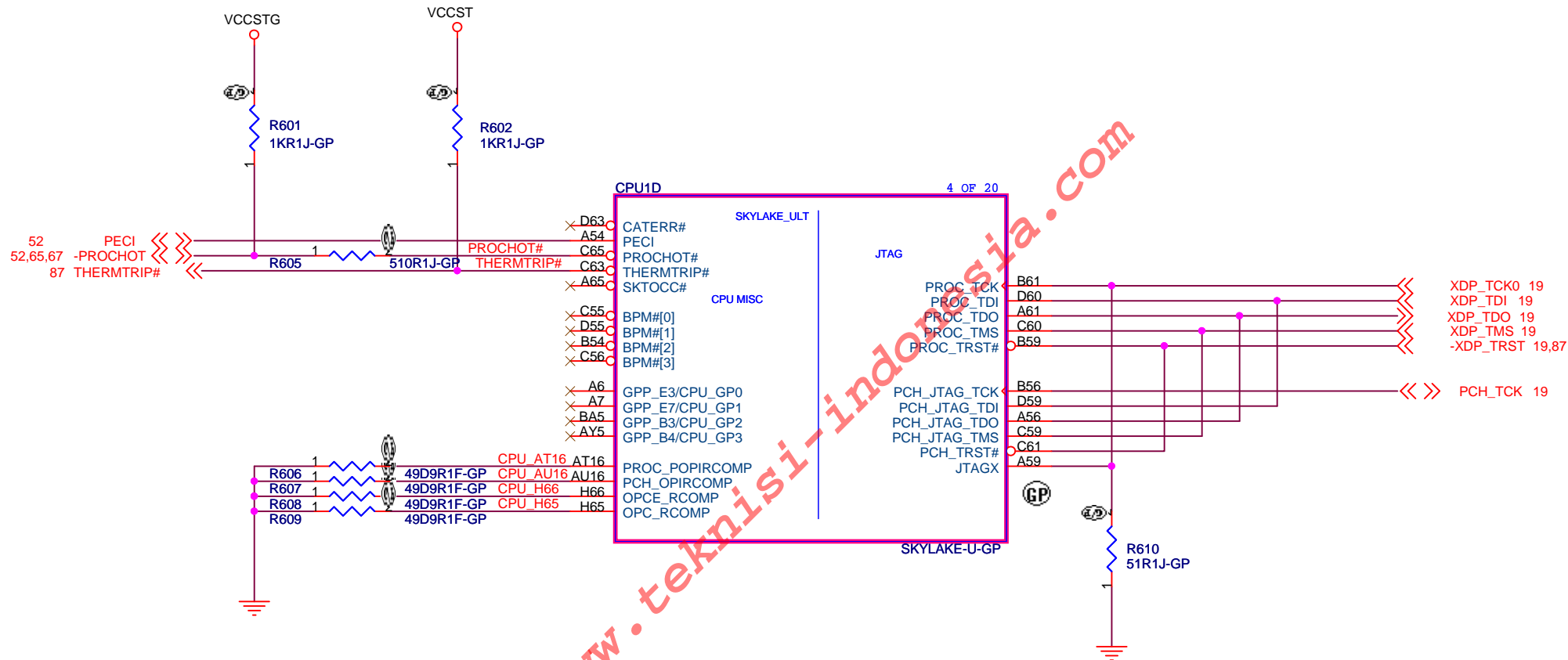
Symbol name	Value	Tolerance (M: +/-20, K: +/-10, Z: +80/-20)	Rating	Size 2=>0402, 3=>0603, 5=>0805 6=>1206, 0=>1210
SCD1U10V2MX-1	0.1uF	M/X5R	10V	0402
SC10U6D3V5MX	10uF	M/X5R	6.3V	0805
SC2D2U16V5ZY	2.2uF	Z/Y5V	16V	0805

The naming rule is
Capacitor type + value + rating + size + tolerance + material
SCD1U10V2MX-1
SC=> SMT Ceramic, TC=> POS cap or SP cap
D1U => 0.1uF
10V => the voltage rating is 10V
2=> 0402, 3=>0603, 5=>0805
M=>tolerance M, K, Z
X=> X7R/X5R, Y=> Y5V
-1 => symbol version, nonsense to EE characteristic

ULT

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Title Description	
Size A4	Document Number <div>Raven-2</div>
Date: Wednesday, April 27, 2016	Rev SA
Sheet 2 of 89	





ULT

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Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title **CPU(4/16) : MISC/JTAG**

Size
A4

Document Number

Raven-2

Rev
SA

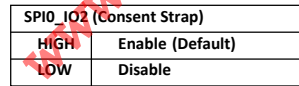
Date: Thursday, May 05, 2016

Sheet 6 of 89

GPP_C5/SMLOALERT# (LPC or eSPI)	
HIGH	eSPI is selected
LOW	LPC is selected (Default)



GPP_C2/SMBALERT# (TLS Confidentiality)	
HIGH	Enable ME Crypto TLS with Confidentiality
LOW	Disable ME Crypto TLS (Default)



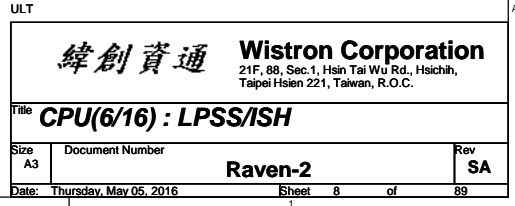
SPI0_MOSI (Boot Halt)	
HIGH	Disable(Default)
LOW	Enable

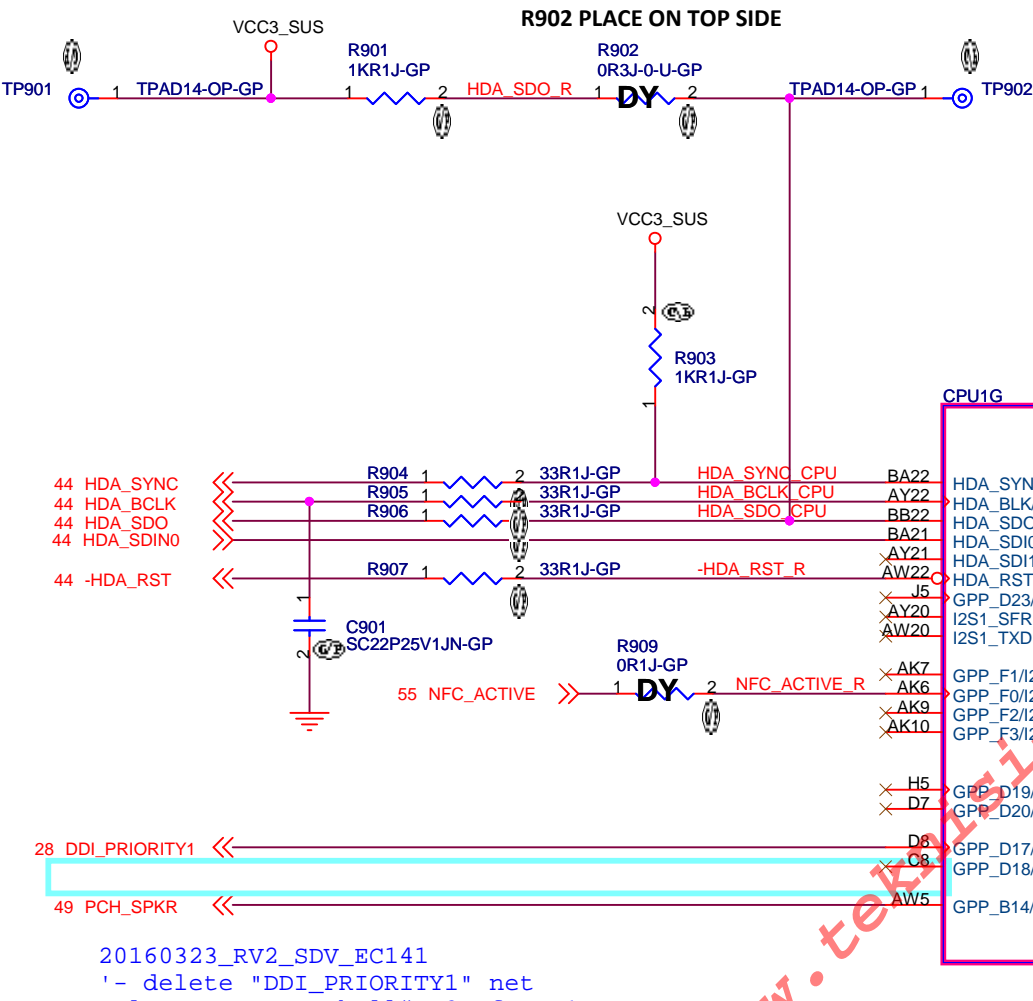
SPI0_IO3 (A0 Personality Strap)	
HIGH	Disable(Default)
LOW	Enable

SPI0_MISO (JTAG ODT Disable)	
HIGH	Enable (Default)
LOW	Disable

GPP_B22/GSPI1_MOSI (Boot BIOS Destination)	
HIGH	Boot BIOS from LPC
LOW	Boot BIOS from SPI (Default)

GPP_B18/GSPI0_MOSI (No Reboot)	
HIGH	Enable "No Reboot" Mode
LOW	Disable "No Reboot" Mode (Default)





TEST PAD: TP901/TP902
BOTTOM SIDE
DO NOT MOVE AFTER FIX

TABLE: Functional Strap

HDA_SDO/I2S0_TXD	
Flash Descriptor Security Override	
HIGH	Disable Flash Descriptor Security (Override)
LOW	Enable Flash Descriptor Security (Default)

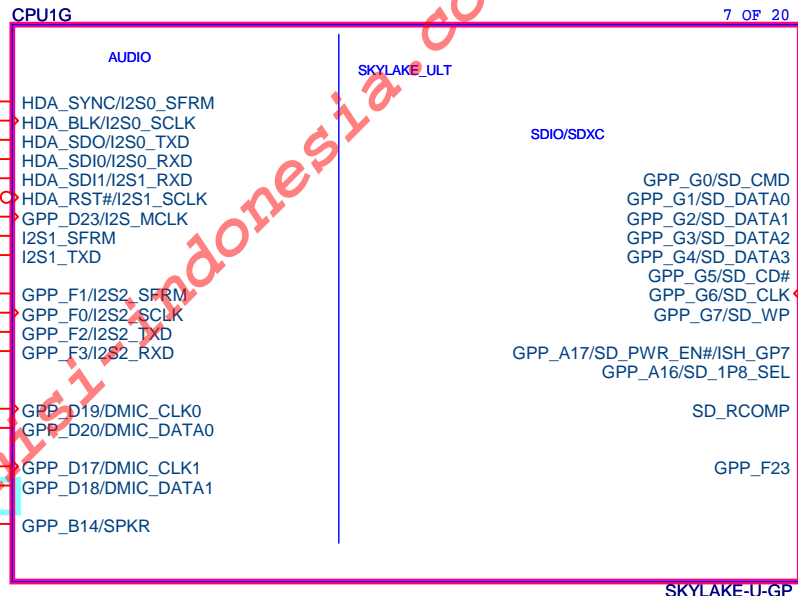


TABLE: Functional Strap

GPP_B14/SPKR (Top Swap Override)	
HIGH	Enable "Top Swap" Mode
LOW	Disable "Top Swap" Mode (Default)

← LOGIC

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TitleCPU(7/16) : AUDIO/SDXC

SizeA4

Document Number

Raven-2

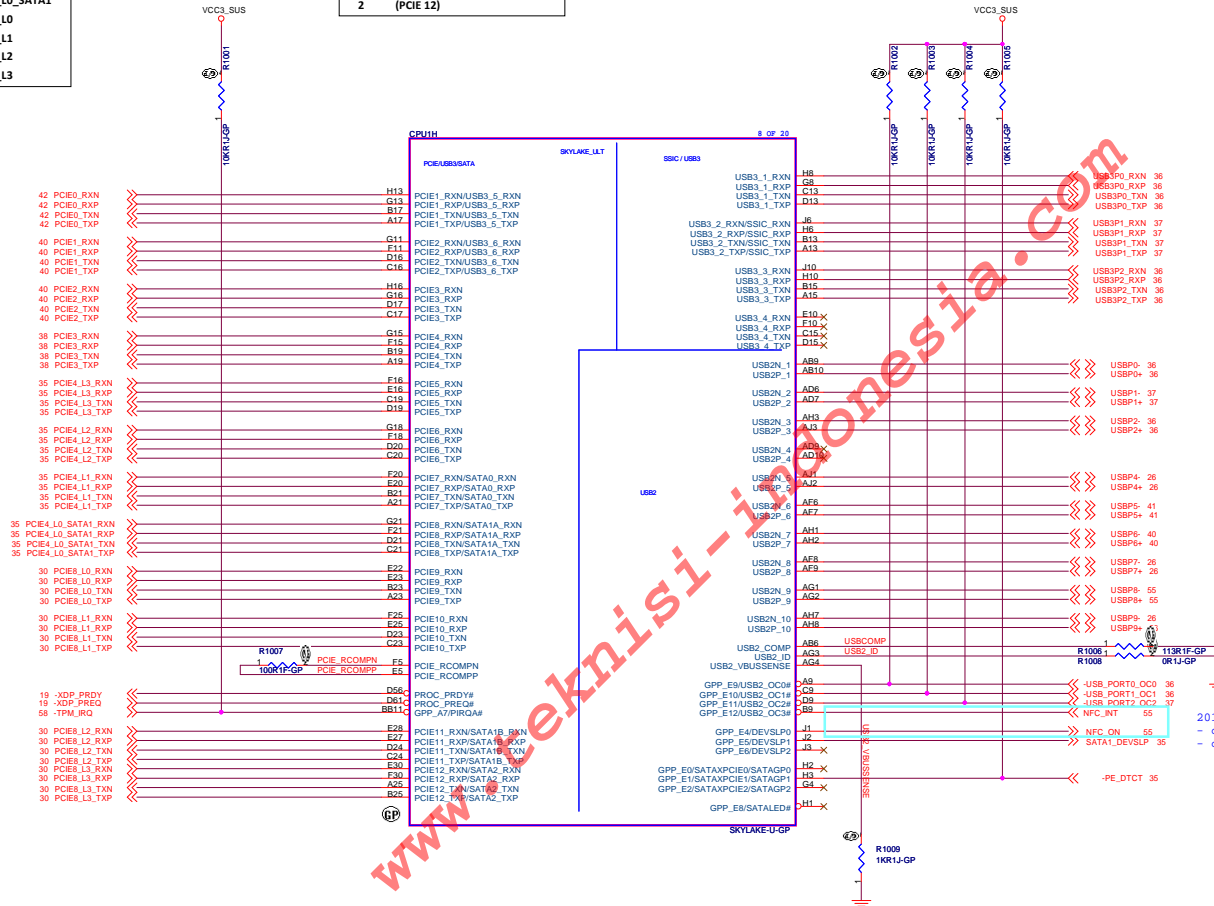
RevSA

Date: Thursday, May 05, 2016Sheet 9 of 89

Flexible I/O Configuration			
I/O	High Speed Signals	Configuration	Net Name
Port 1	USB3 1	USB3 1	USB3P0
Port 2	USB3 2/SSIC	USB3 2	USB3P1
Port 3	USB3 3	USB3 3	USB3P2
Port 4	USB3 4	USB3 4	N/A
Port 5	USB3 5/PCIE 1	PCIE 1	PCIE0
Port 6	USB3 6/PCIE 2	PCIE 2	PCIE1
Port 7	PCIE 3 (GbE)	PCIE 3	PCIE2
Port 8	PCIE 4 (GbE)	PCIE 4 (GbE)	PCIE3
Port 9	PCIE 5 (GbE)	PCIE 5 (x4)	PCIE4_L3
Port 10	PCIE 6	PCIE 6 (x4)	PCIE4_L2
Port 11	PCIE 7/SATA 0	PCIE 7 (x4)	PCIE4_L1
Port 12	PCIE 8/SATA 1A	GPIO STRAP	PCIE4_L0_SATA1
Port 13	PCIE 9 (GbE)	PCIE 9 (x4)	PCIE8_L0
Port 14	PCIE 10 (GbE)	PCIE 10 (x4)	PCIE8_L1
Port 15	PCIE 11/SATA 1B	PCIE 11 (x4)	PCIE8_L2
Port 16	PCIE 12/SATA 2	PCIE 12 (x4)	PCIE8_L3

PCIe Port Assignment	
0	Media Card Controller
1	M.2 WLAN Slot Port 1 for WiGig
2	M.2 WLAN Slot Port 0 for WLAN
3	GbE PHY
4 (x4)	PCIe SSD
8 (x4)	Thunderbolt

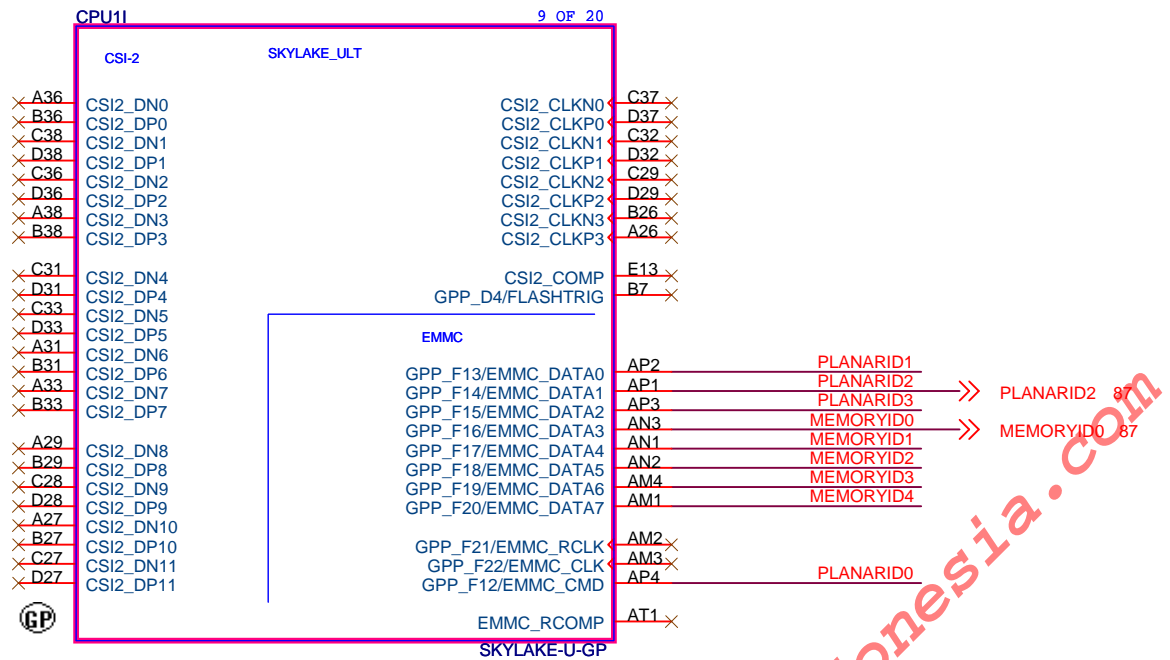
SATA Port Assignment	
0	(PCIE 7)
1A	SATA SSD
1B	(PCIE 11)
2	(PCIE 12)



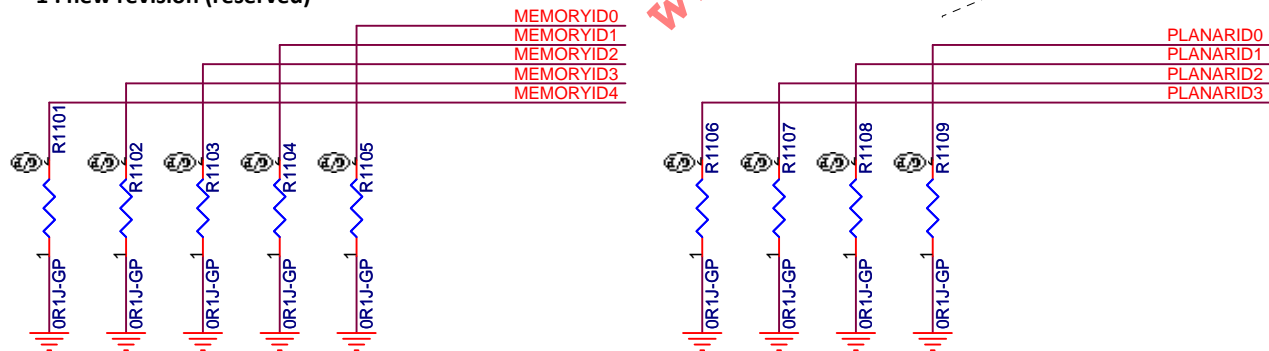
USB 3.0 Port Assignment	
0	USB 3.0 System Port (AOU)
1	USB 3.0 System Port
2	USB 3.0 System Port
3	(Reserved)
4	(PCIE 1)
5	(PCIE 2)

USB Port Assignment	
0	USB 3.0 System Port (AOU)
1	USB 3.0 System Port
2	USB 3.0 System Port
3	(Reserved)
4	IR Camera
5	M.2 WWAN Slot
6	M.2 WLAN Slot for BT
7	USB Camera
8	Fingerprint Reader
9	Touch Panel

20160406_RV2_SDV_EC161
- connect net "NFC_INT" to ball# B9 of CPU1
- connect net "NFC_ON" to ball# J1 of CPU1



MEMORY ID
MEMORYID[4:3] GPP_F[20:19] System Memory Configuration
00 : 4GB dual channel (8Gb x 4pcs) <-- Logic
01 : (Reserved)
10 : 8GB (16Gb x4pcs)
11 : 16GB (32Gb x4pcs)
MEMORYID[2:1] GPP_F[18:17] Memory Supplier
00 : Samsung <-- Logic
01 : Micron
10 : SK Hynix
11 : (Reserved)
MEMORYID0 GPP_F16 Memory Die Revision
0 : initial <-- Logic
1 : new revision (reserved)



TABLE

LEVEL	PLANAR ID			
	3	2	1	0
	R1106	R1107	R1108	R1109
1	NA	NA	NA	NA
0	ASM	ASM	ASM	ASM

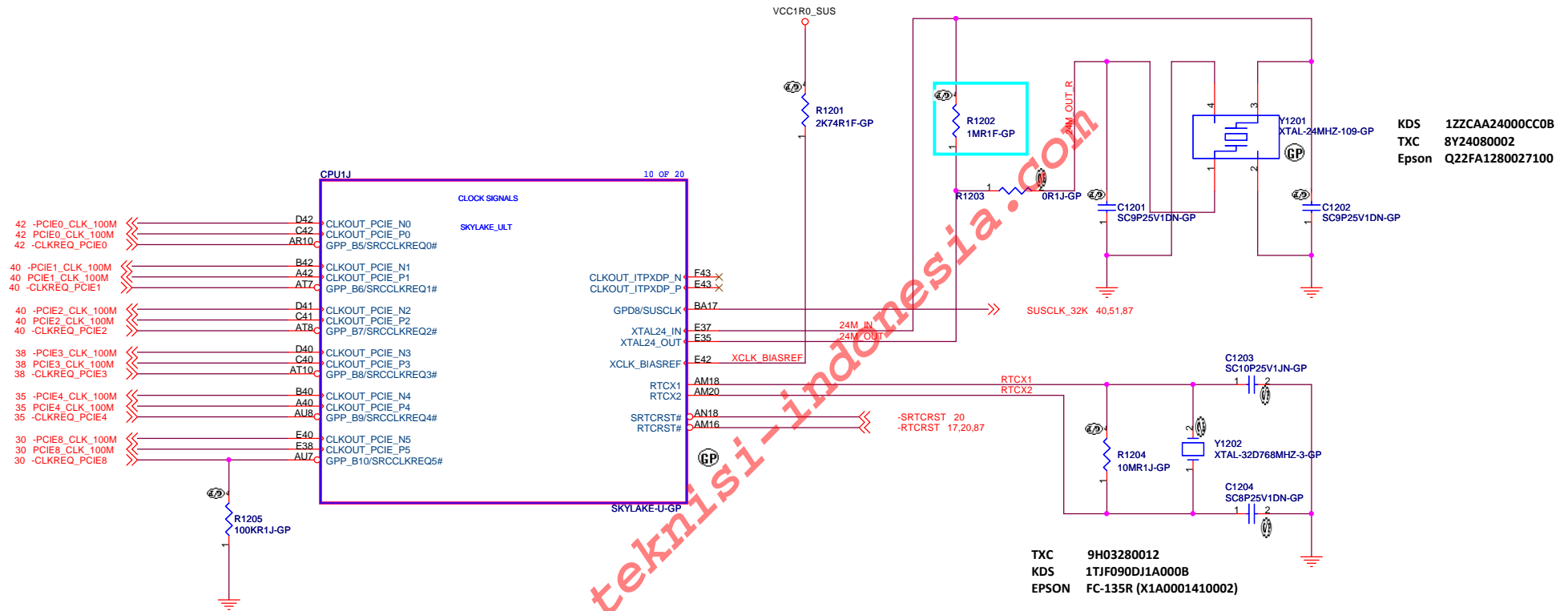
TABLE

LEVEL	PLANARID[3..0]
SDV (SA)	0000B
FVT	
SIT	
SVT	
SOVP	

ULT

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Title CPU(9/16) : CSI-2/EMMC	
Size A4	Document Number Raven-2
Date: Thursday, May 05, 2016	Rev SA
Sheet 11 of 89	

20160406_RV2_SDV_EC170
Change R1202 to 1Mohm 1% 0201



KDS 1ZZCAA24000CC0B
TXC 8Y24080002
Epson Q22FA1280027100

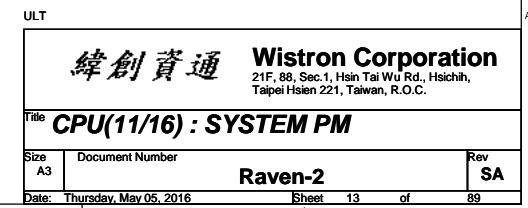
TXC 9H03280012
KDS 1TJF090DJ1A000B
EPSON FC-135R (X1A0001410002)

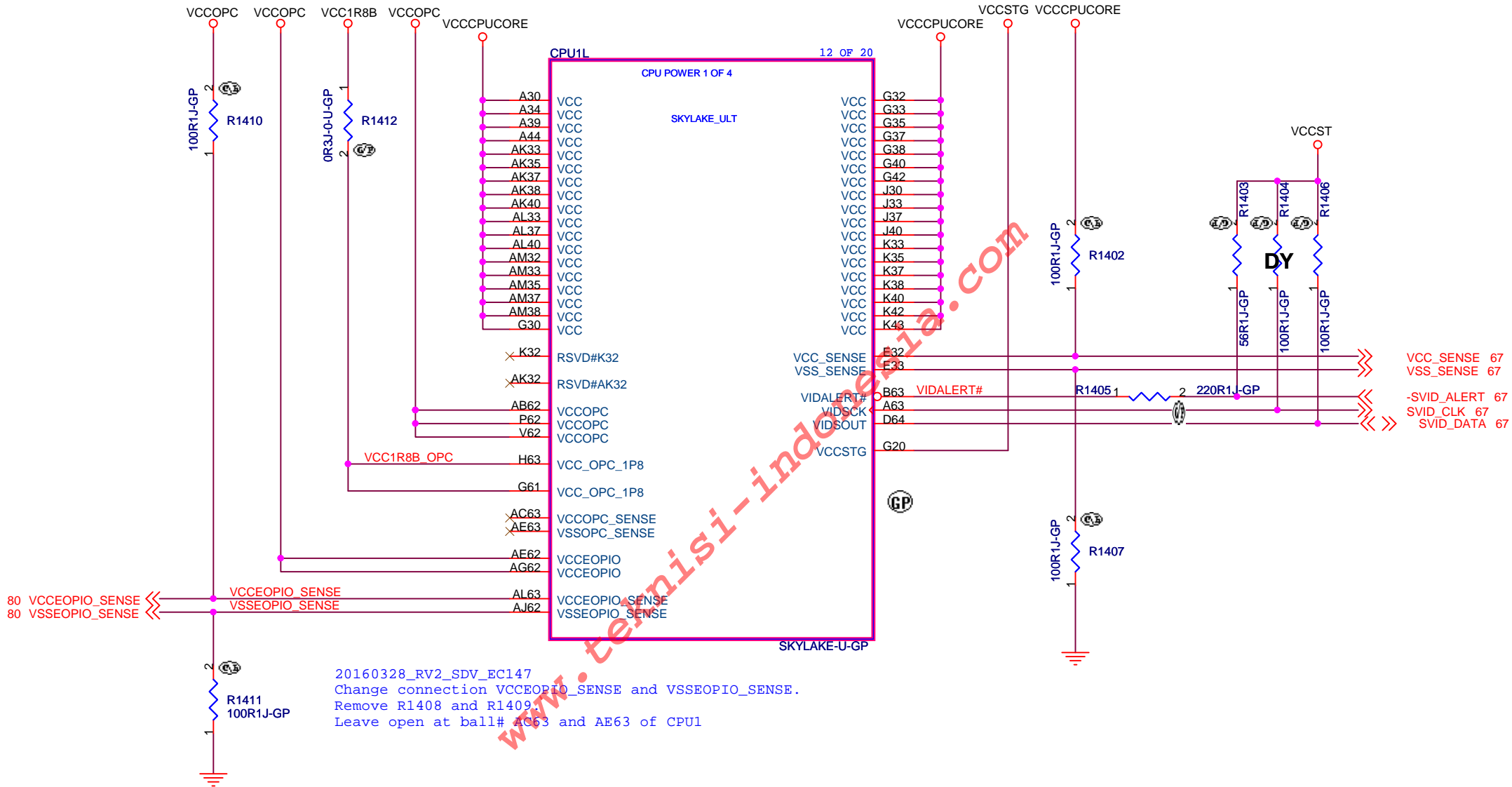
ULT

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Taipei Hsien 221, Taiwan, R.O.C.

Title CPU(10/16) : CLOCK SIGNALS

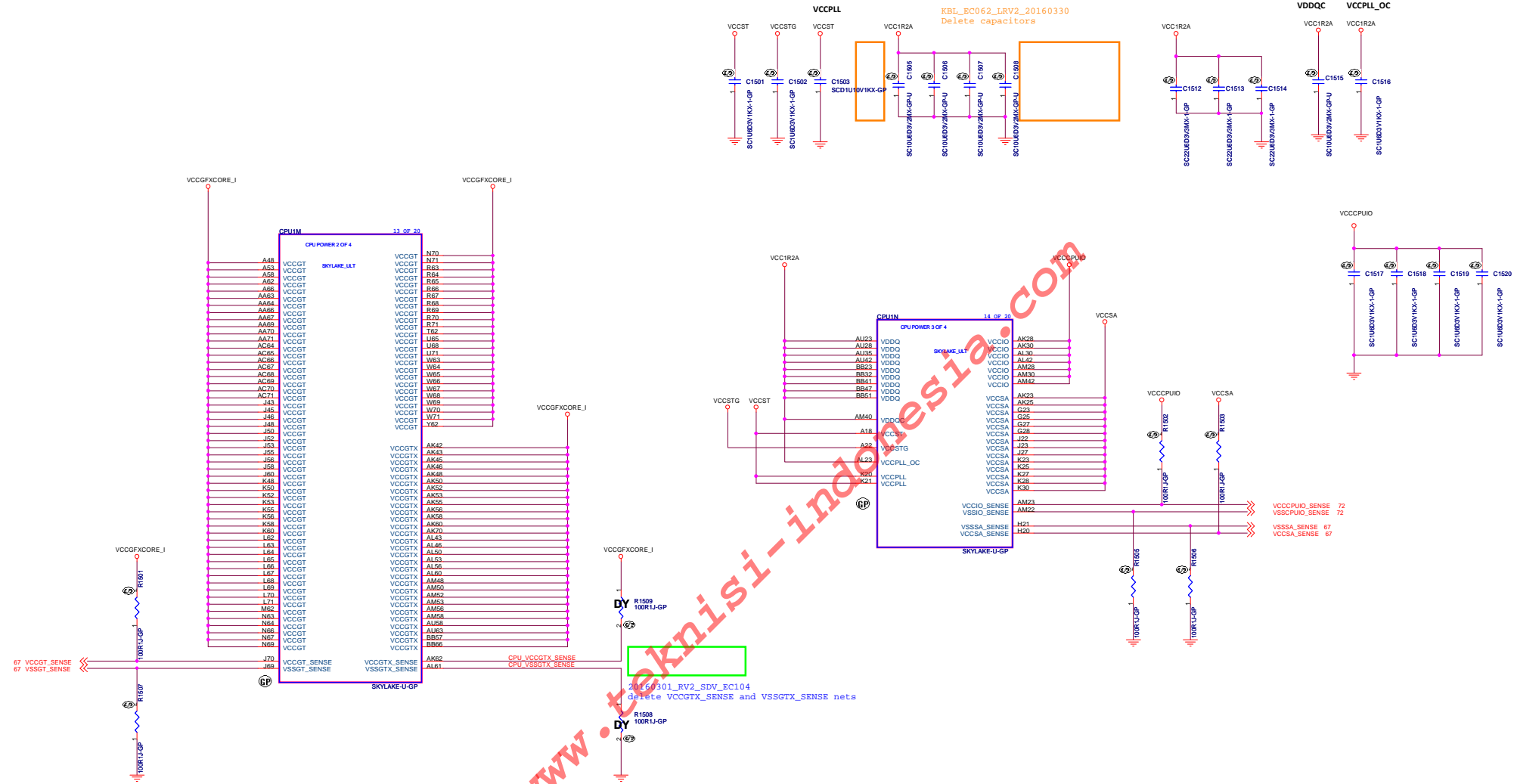
Size A3	Document Number	Rev SA
Date: Thursday, May 05, 2016		Sheet 12 of 89

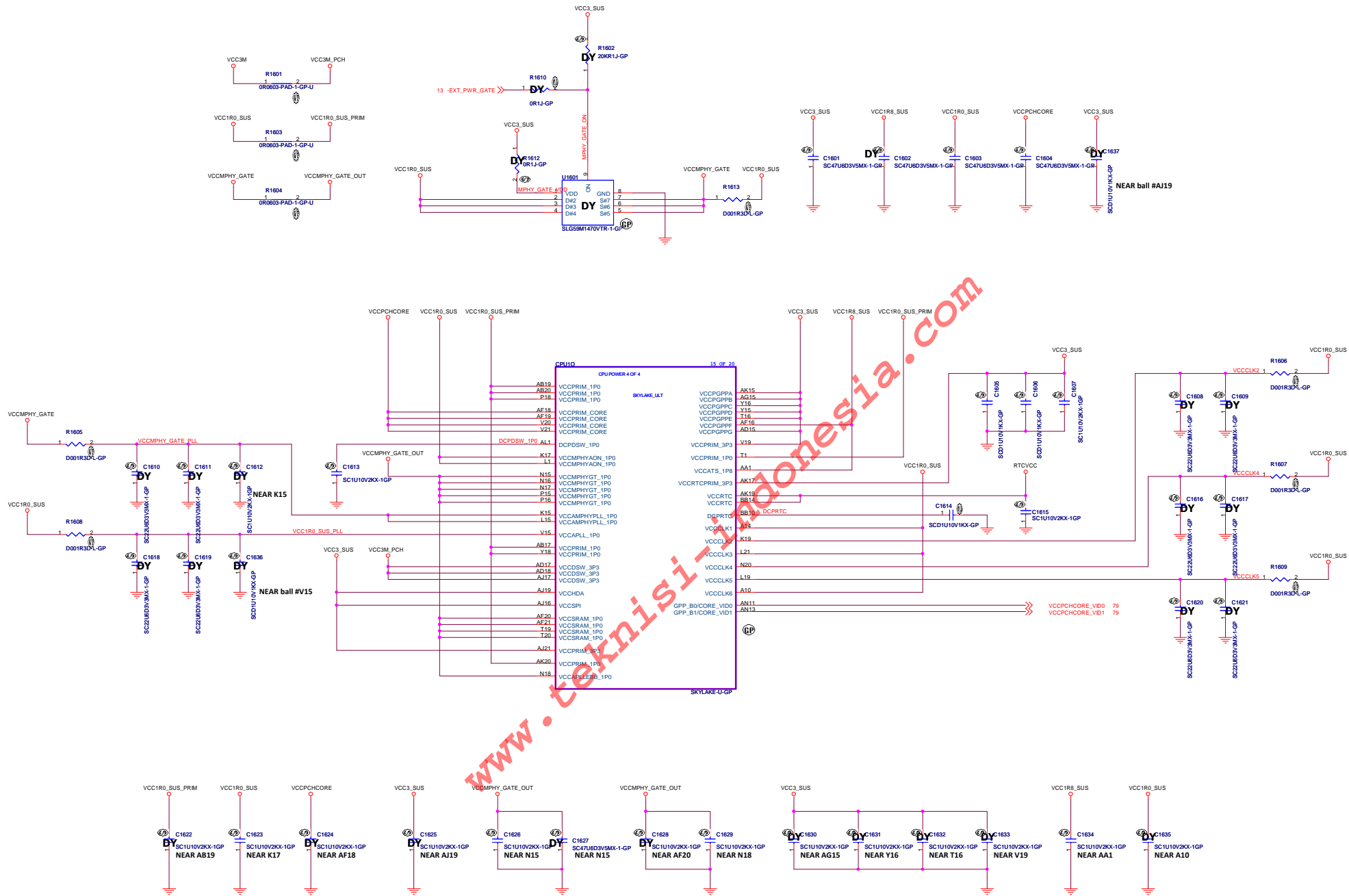


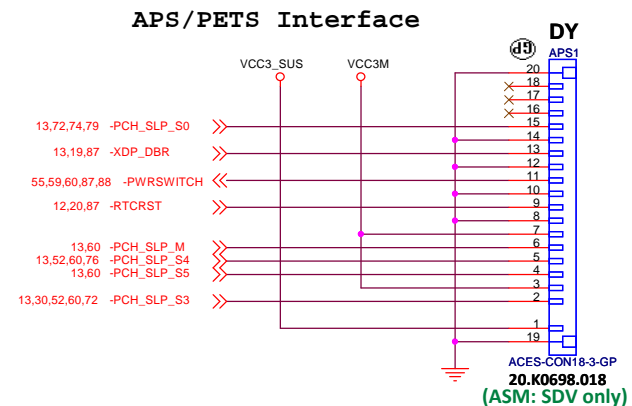
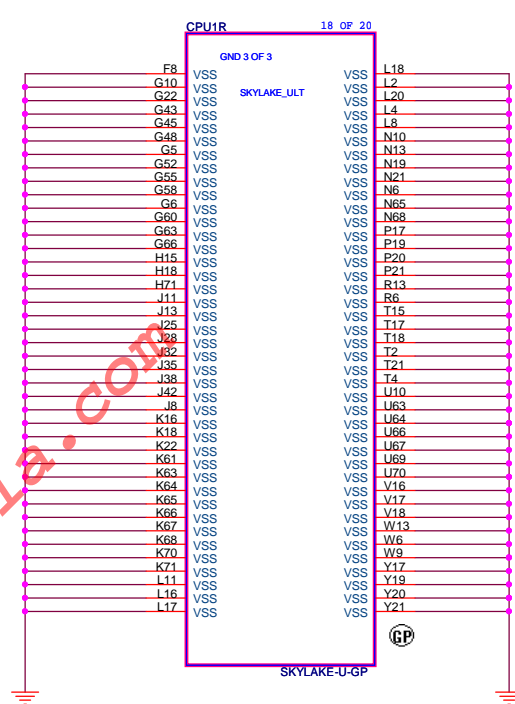
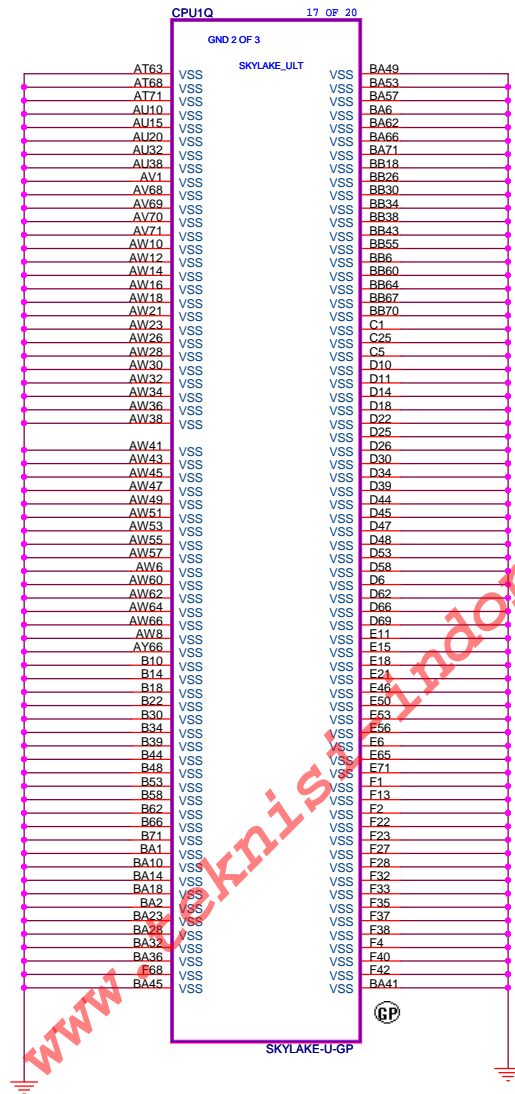
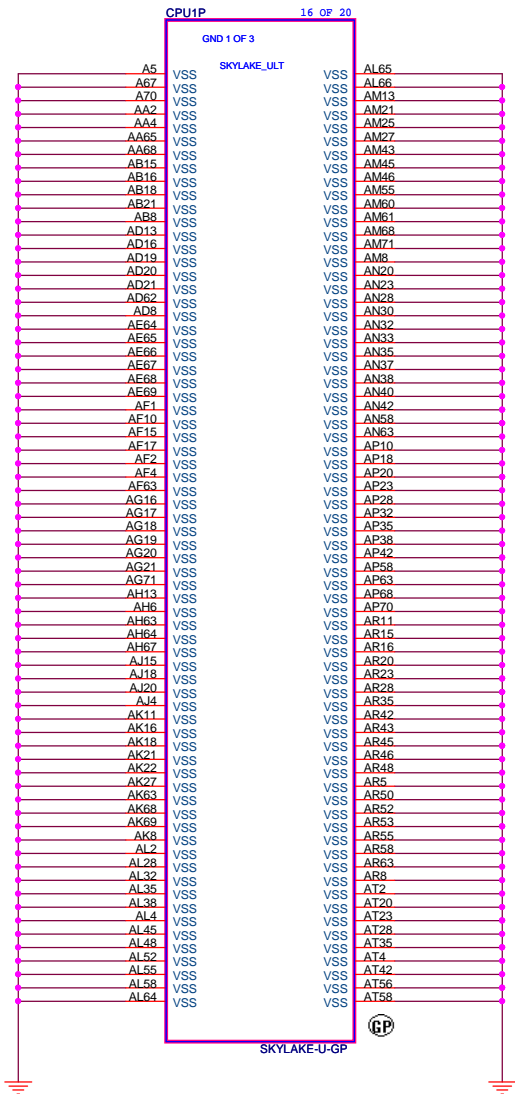


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Title CPU(12/16) : CPU POWER(1/2)		
Size A4	Document Number Raven-2	Rev SA
Date: Thursday, May 05, 2016		Sheet 14 of 89







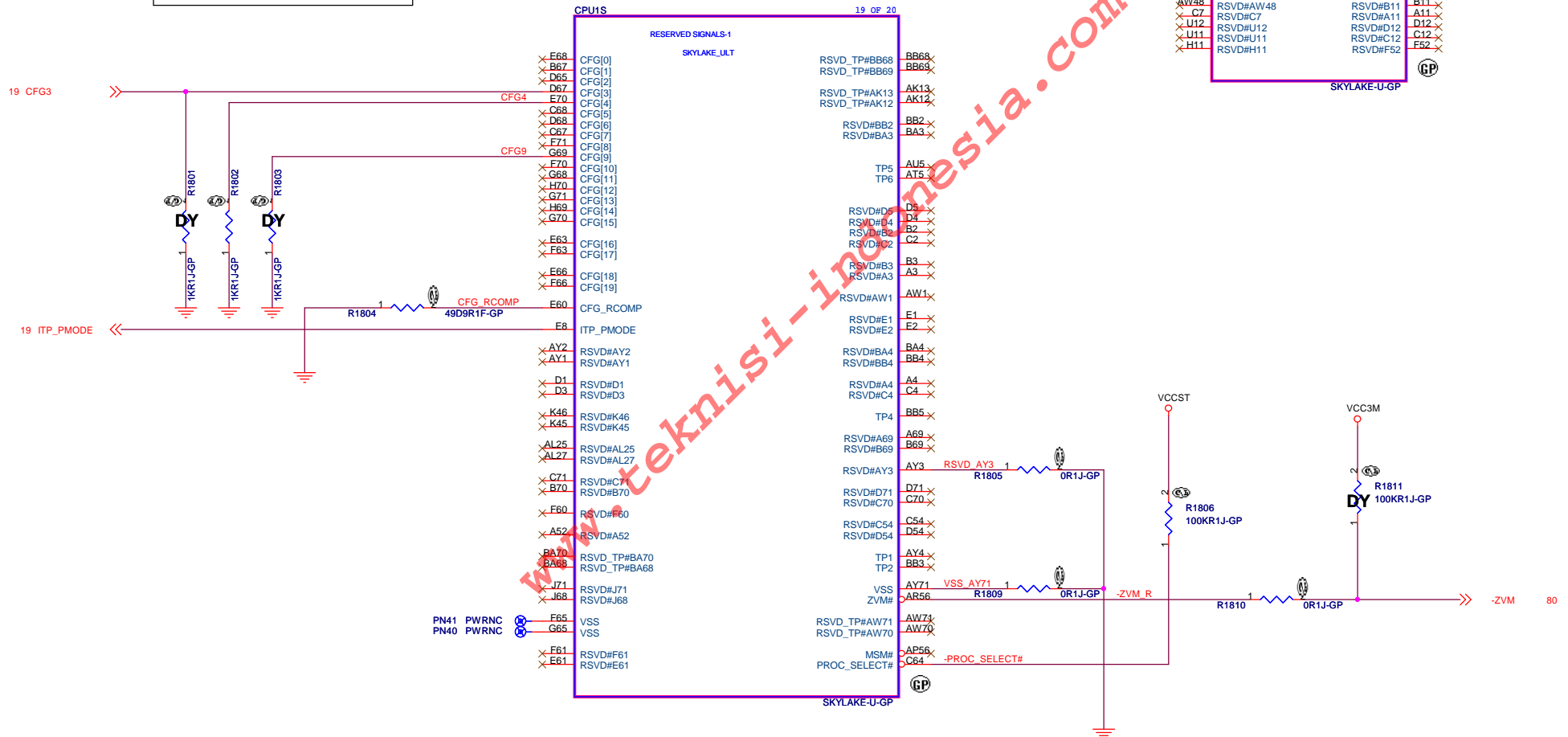
TABLE

**CFG0 : Stall Reset Sequence
after PCU PLL Lock until de-asserted**
1 : No Stall
0 : Stall

CFG3 : MSR Privacy Bit Feature
1 : MSR (C80h) bit[0] setting
0 : MSR (C80h) bit[0] overridden

CFG4 : eDP Enable
1 : Disabled
0 : Enabled

CFG9 : SVID Bus Communication
1 : Enabled
0 : Disabled

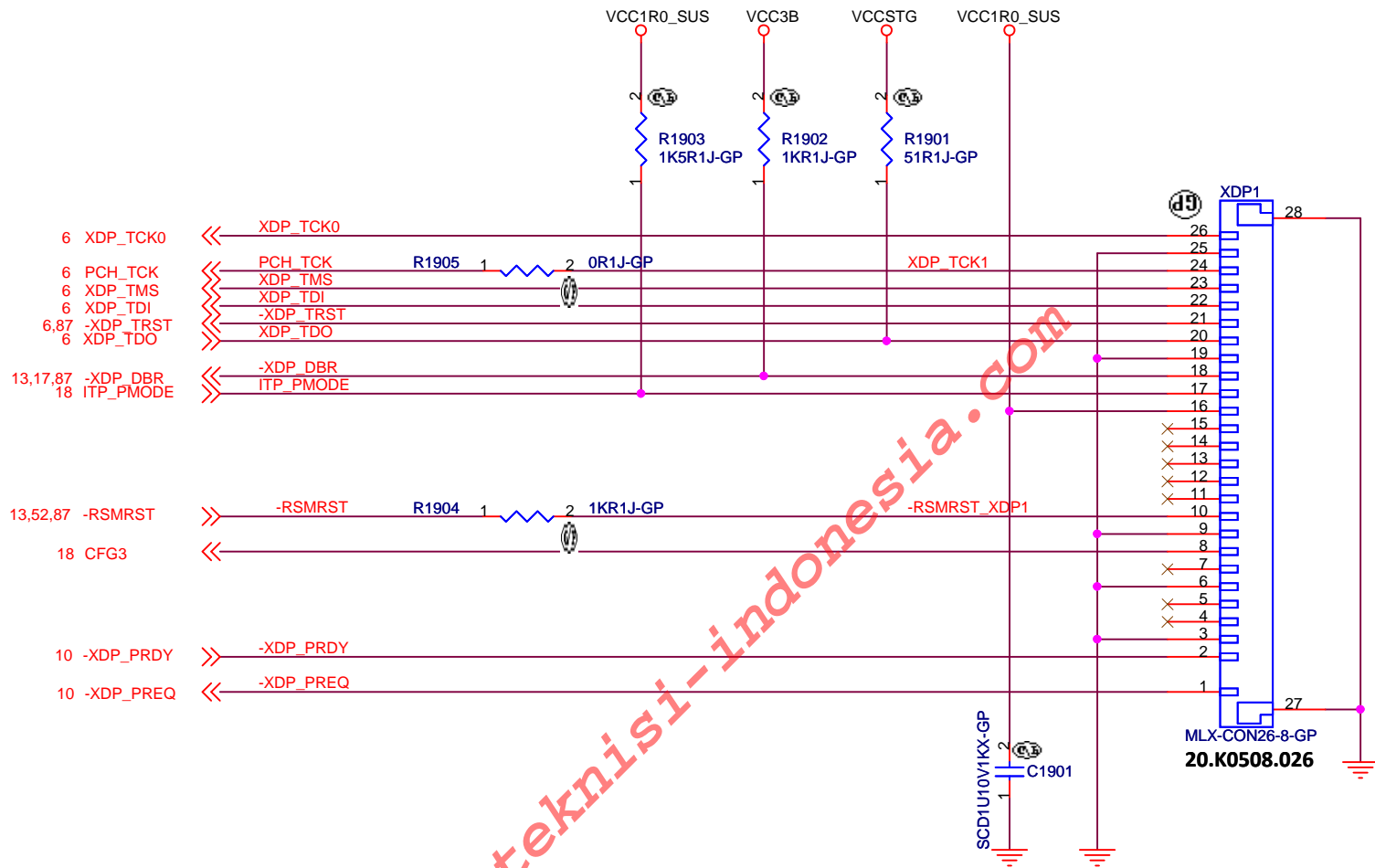


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Title **CPU(16/16) : CFG/RESERVED**

Size A3	Document Number Raven-2	Rev SA
Date: Thursday, May 05, 2016	Sheet 18 of 89	



Logic	Ref Des	Merged	DCI2.0
Page 7	R711	ASM	NOASM
Page 18	R1801	ASM	NOASM
Page 19	XDP1	ASM	NOASM
	C1901	ASM	NOASM
	R1901	ASM	ASM
	R1902	ASM	ASM
	R1903	ASM	NOASM
	R1904	ASM	NOASM
	R1905	ASM	NOASM

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Title

XDP CONNECTOR

Size
A4

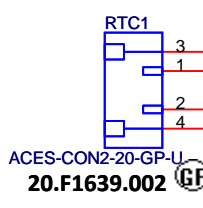
Document Number
Raven-2

Rev
SA

Date: Thursday, May 05, 2016

Sheet 19 of 89

RTC CONN



RTCVCC_CONN

R2001
1KR1J-GP



1 2

RTCVCC_D

D2001
RB520CM-30T2R-GP



A K

VCC3SW

D2003
RB520CM-30T2R-GP



A K

D2002
RB520CM-30T2R-GP



A K

RTCVCC

C2002
SC1U6D3V1KX-1-GP



R2002
20KR1J-GP



1 2

-RTCRST 12,17,87

C2001
SC1U6D3V1KX-1-GP



R2003
20KR1J-GP



1 2

-SRTCST 12

C2003
SC1U6D3V1KX-1-GP



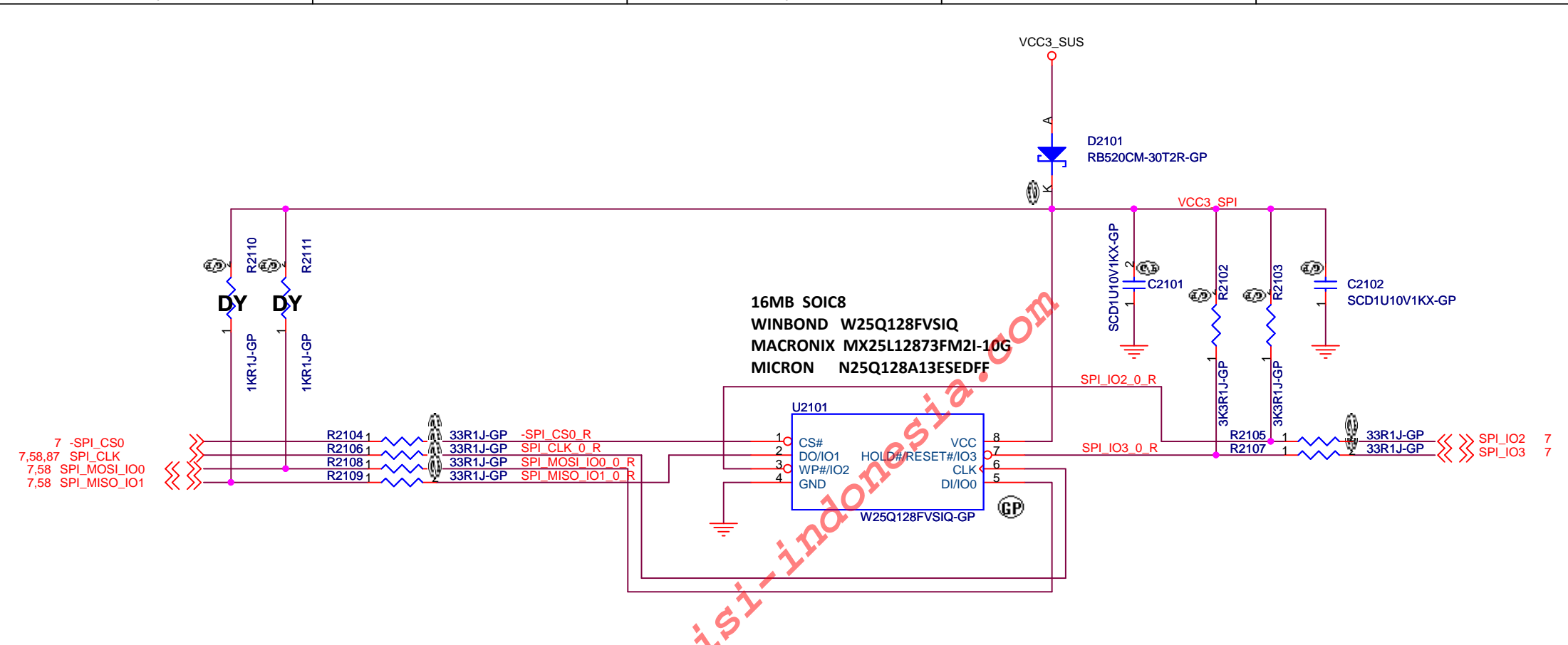
ULT

緯創資通

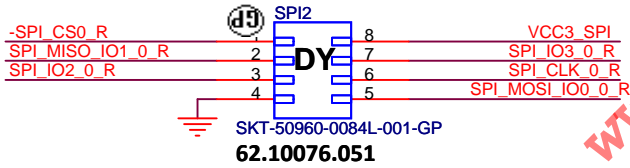
Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title **RTC BATTERY**

Size A4	Document Number Raven-2	Rev SA
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SPI ROM Socket (SPI2)



Co-Layout Design on U2101
(ASM: SDV only)

TABLE

SF100 PIN HEADER INTERFACE (TOP VIEW)							
1	VCC	D2101.K	GND	GND	2		
3	CS#	R2104.2	R2106.2	CLK	4		
5	MISO	R2109.2	R2108.2	MOSI	6		
7	(KEY)	N/A	N/A	(RESET)	8		

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Title

SPI FLASH

Size

Document Number

Rev

SA

Date

Thursday, May 05, 2016

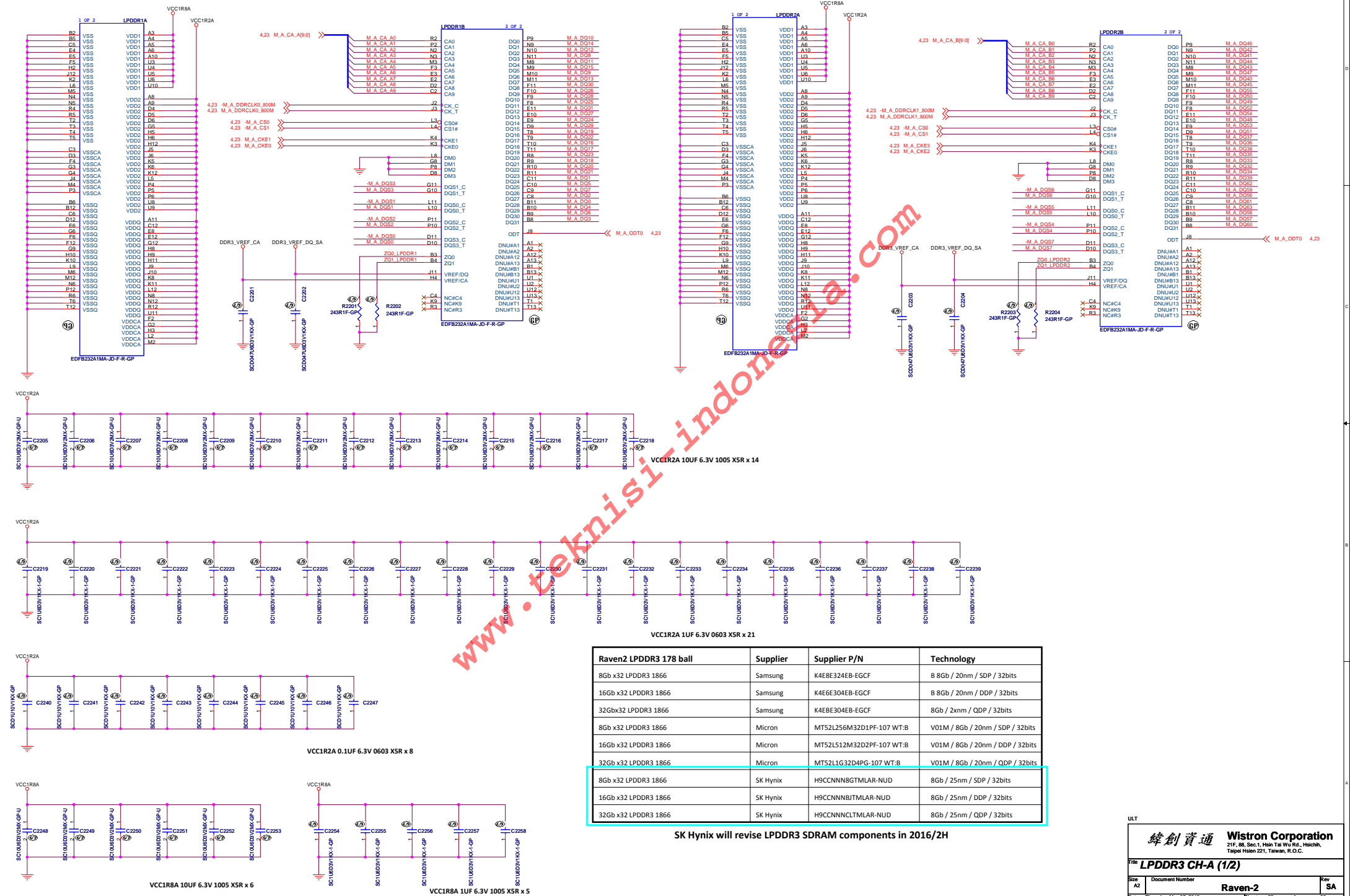
Sheet

21

of

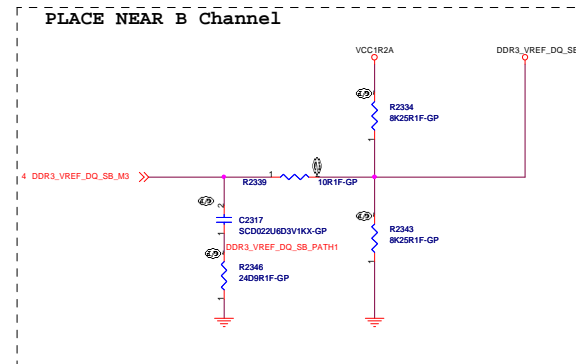
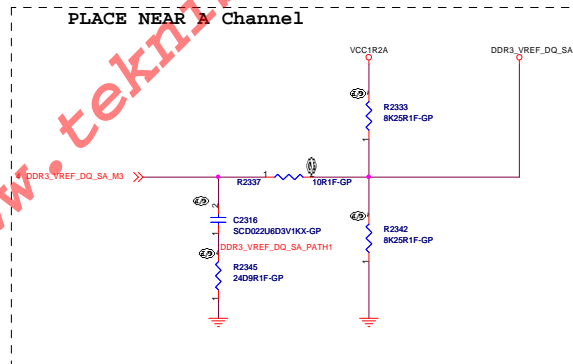
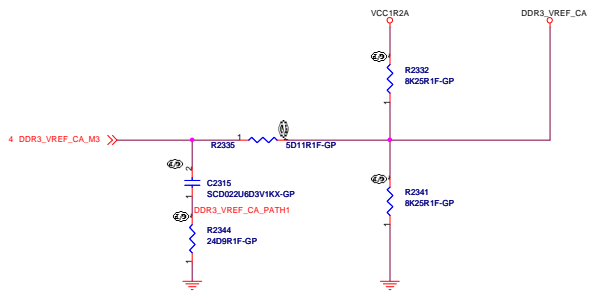
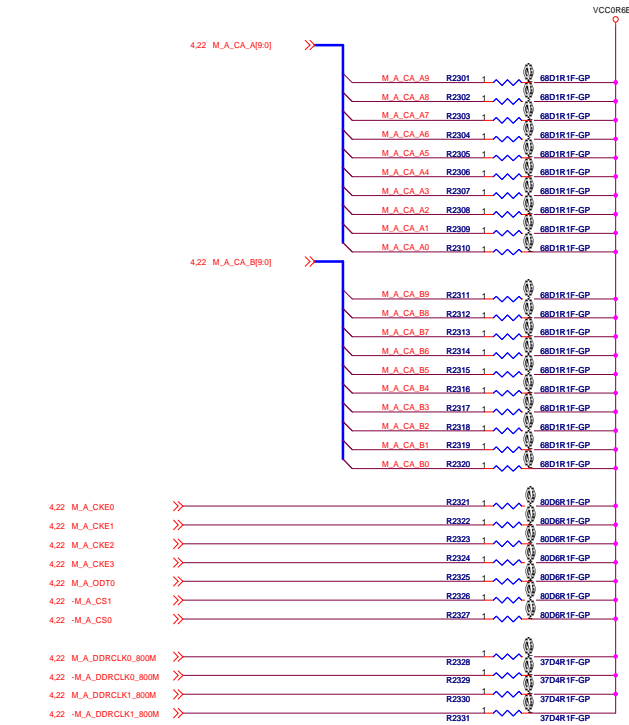
89

4 M_A_DQ[3:0] << >>
4 -M_A_DQ[5:7] << >>
4 M_A_DQ[8:7] << >>

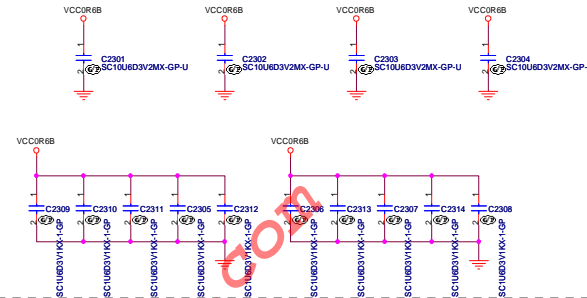


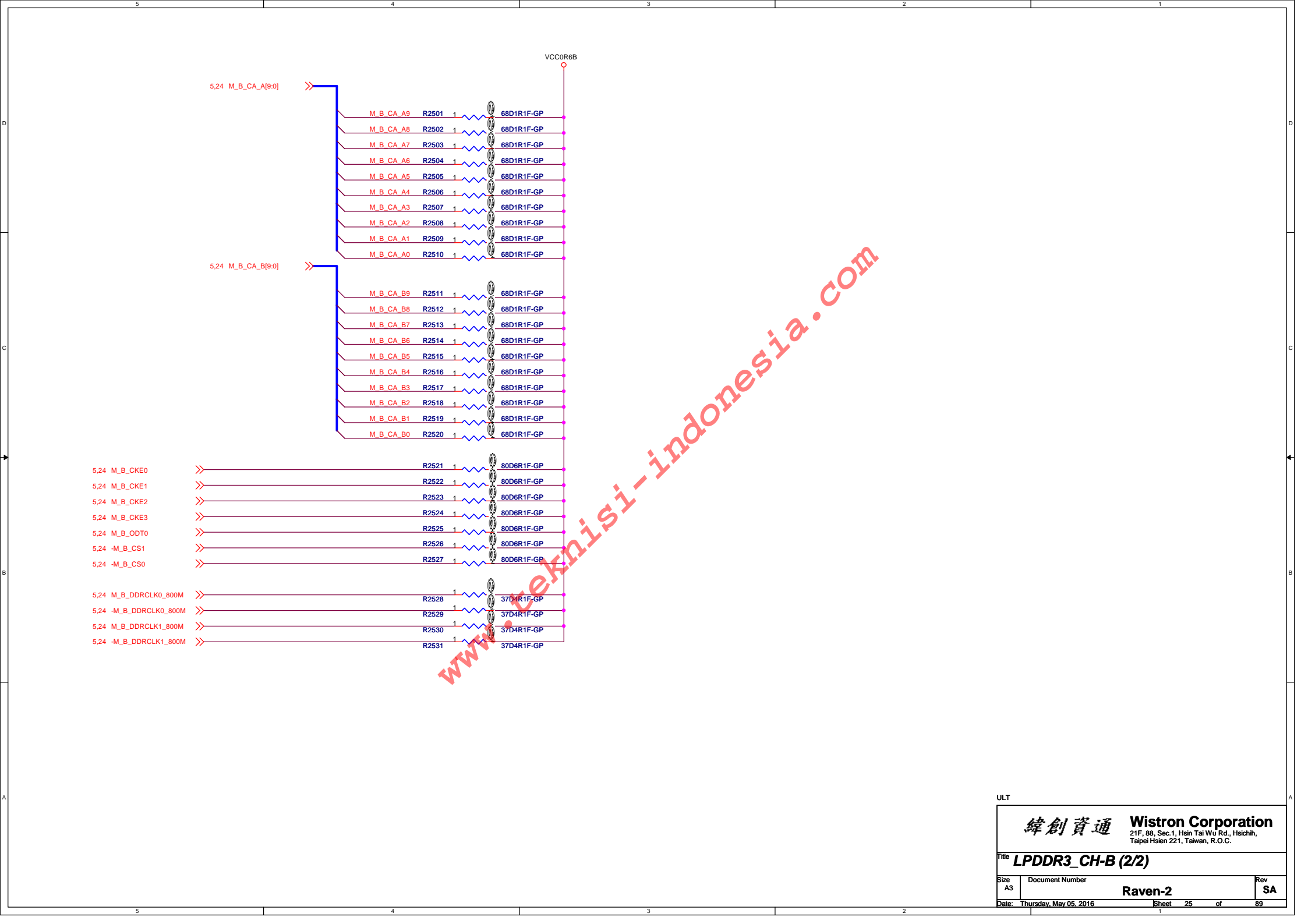
Raven2 LPDDR3 178 ball	Supplier	Supplier P/N	Technology
8Gb x32 LPDDR3 1866	Samsung	K4E8E324EB-EGCF	B 8Gb / 20nm / SDP / 32bits
16Gb x32 LPDDR3 1866	Samsung	K4E6E304EB-EGCF	B 8Gb / 20nm / DDP / 32bits
32Gb x32 LPDDR3 1866	Samsung	K4E8E304EB-EGCF	8Gb / 2nm / QDP / 32bits
8Gb x32 LPDDR3 1866	Micron	MT52L256M32D1PF-107 WT:B	V01M / 8Gb / 20nm / SDP / 32bits
16Gb x32 LPDDR3 1866	Micron	MT52L512M32D2PF-107 WT:B	V01M / 8Gb / 20nm / DDP / 32bits
32Gb x32 LPDDR3 1866	Micron	MT52L1G32D4PG-107 WT:B	V01M / 8Gb / 20nm / QDP / 32bits
8Gb x32 LPDDR3 1866	SK Hynix	H9CCNNN8GTMLAR-NUD	8Gb / 25nm / SDP / 32bits
16Gb x32 LPDDR3 1866	SK Hynix	H9CCNNNB/TMLAR-NUD	8Gb / 25nm / DDP / 32bits
32Gb x32 LPDDR3 1866	SK Hynix	H9CCNNNCLTMLAR-NUD	8Gb / 25nm / QDP / 32bits

SK Hynix will revise LPDDR3 SDRAM components in 2016/2H



LPDDR3 Vtt Decoupling





ULT



20160408_RV2_SDV_EC175
'- delete all circuit in page 27

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ULT

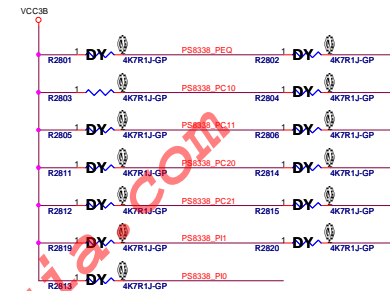
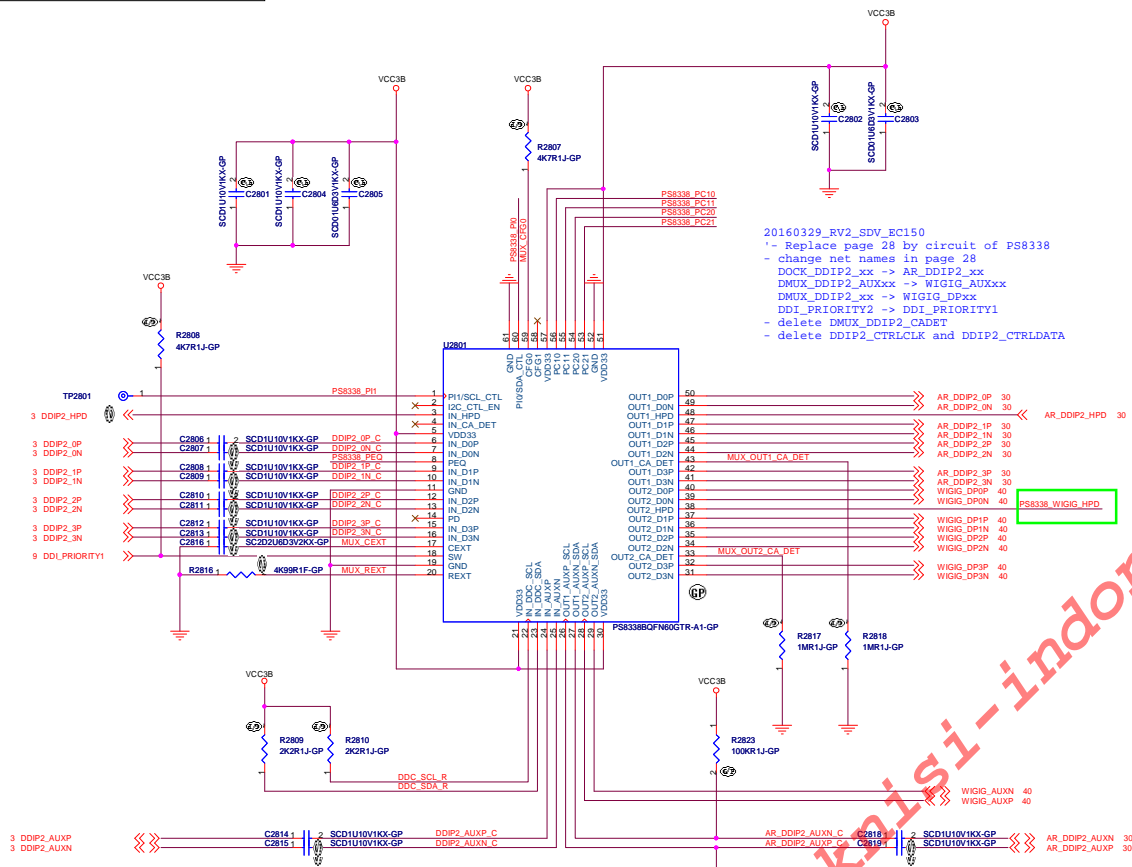
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		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title BLANK			
Size A4	Document Number Raven-2		Rev SA
Date: Thursday, May 05, 2016		Sheet 27 of	89

TABLE : Automatic Switching Mode (CFG0 = H)

SW (DDI_PRIORITY1)

L AR has higher priority when both ports are plugged

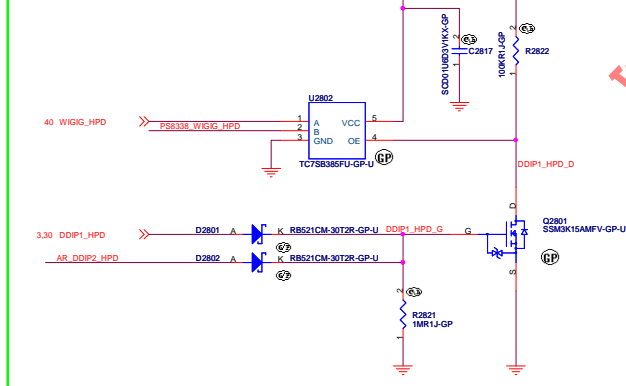
H WIGIG Port has higher priority when both ports are plugged



20160411_RV2_SDV_EC180

'- add bus switch circuit to page 28

- change net name to PS8338_WIGIG_HP

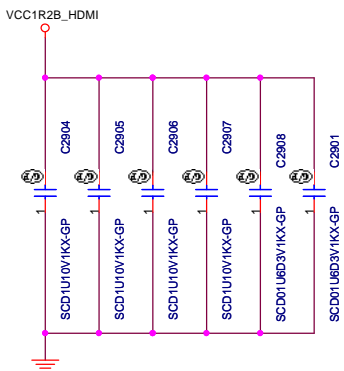
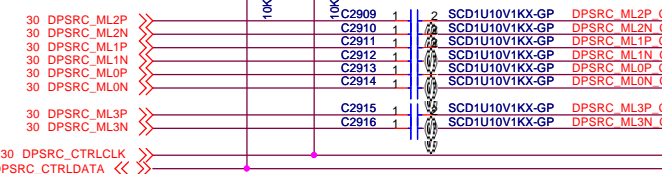
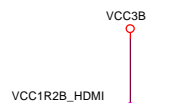
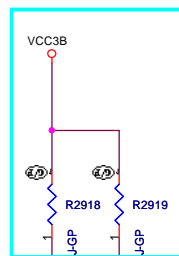
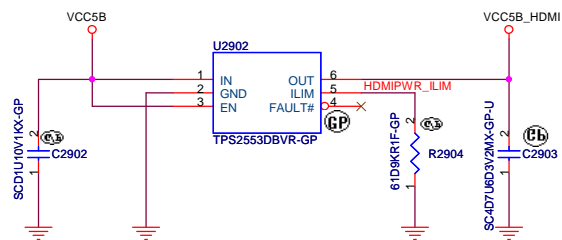


ULT

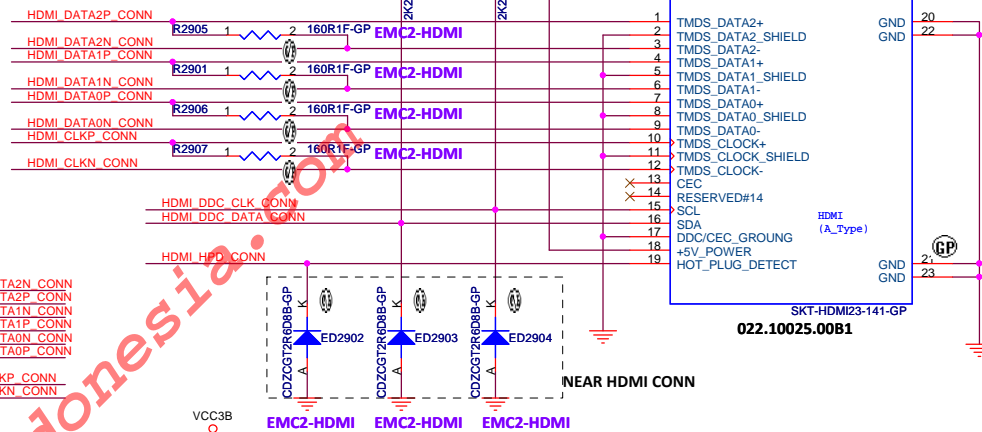
U2902

main TI TPS2553DBVR
2nd GMT G517AL1TB1U

Current Limit Target : 400mA
Requirement : 350mA
HDMI Spec : 50mA - 500mA



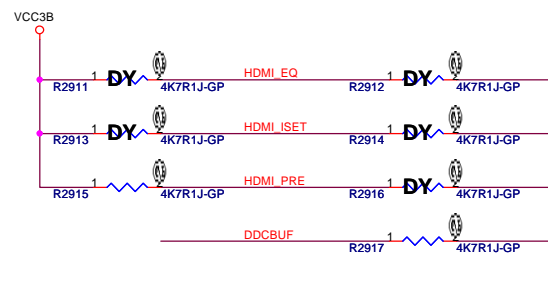
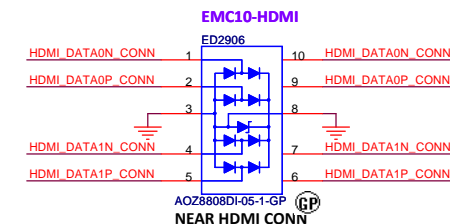
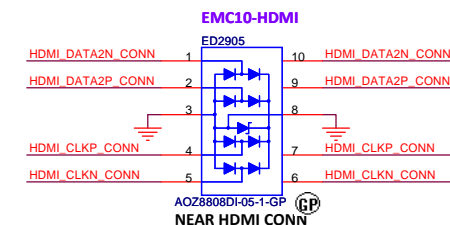
20160329_RV2_SDV_EC150
- connect DPSRC_MLxx to DP input of U2901 via 0.1uF
- connect DPSRC_CTRLCLK and DPSRC_CTRLCLK to SDA port of U2901 with 10Kohm pull-up resistors
- DPSRC_HPD connect to pin#3 of U2901



No need diode here because TPS2553 has reverse voltage protection function.

TABLE OF TVS DIODE: D2905,D2906

	Vendor	Vendor P/N	Wistron P/N
1st	AOS	AOZ8808DI-05	75.08808.073
2nd	SEMTECH	RClamp0524PATCT	75.00524.073
3rd			

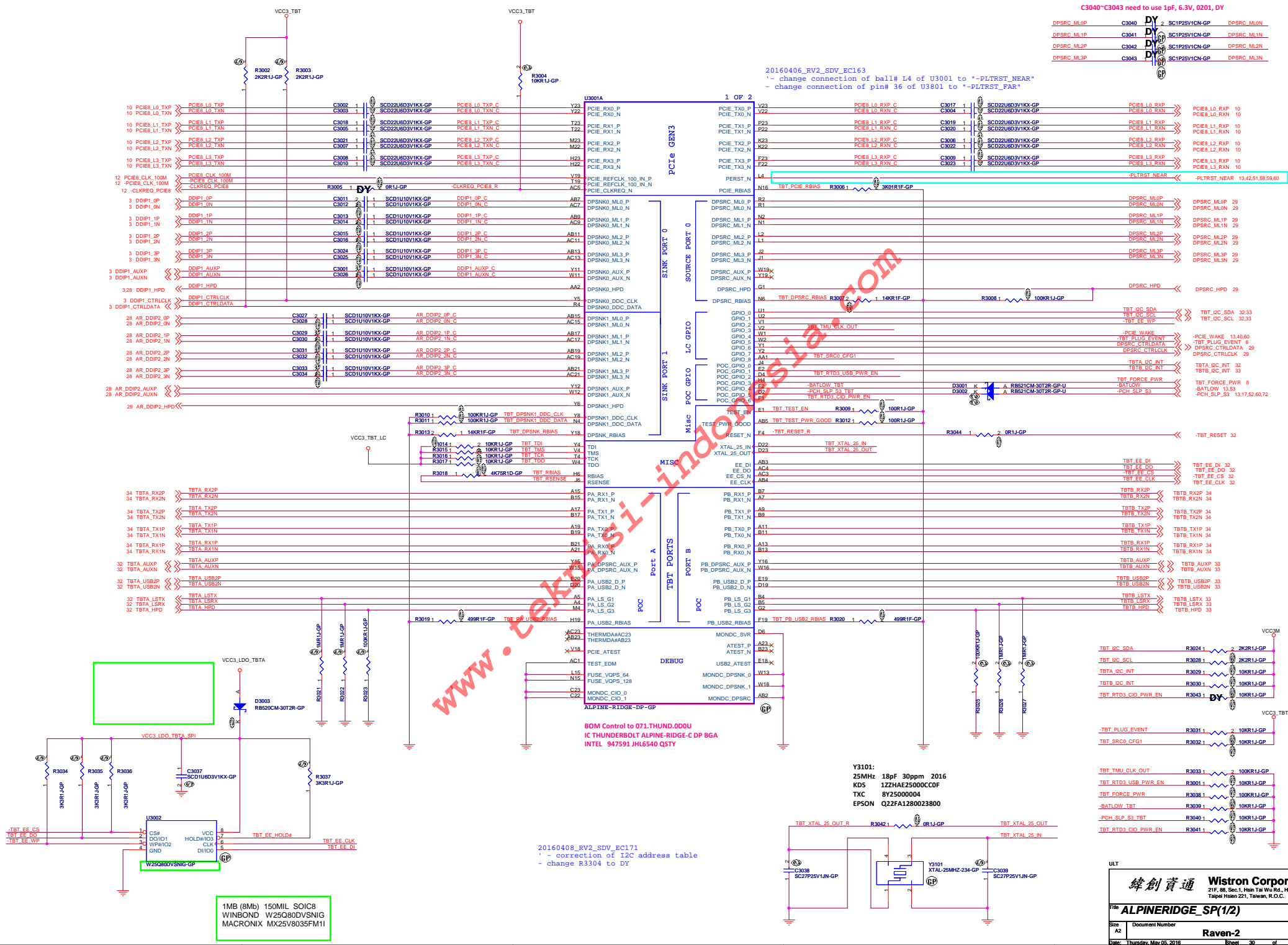


ULT

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title HDMI CONNECTOR

Size A3 Document Number Raven-2 Rev SA
Date: Thursday, May 05, 2016 Sheet 29 of 89



```
20160204_RV2_SDV_EC066
Change power net from VCC3_SUS to VCC3_TBT
```



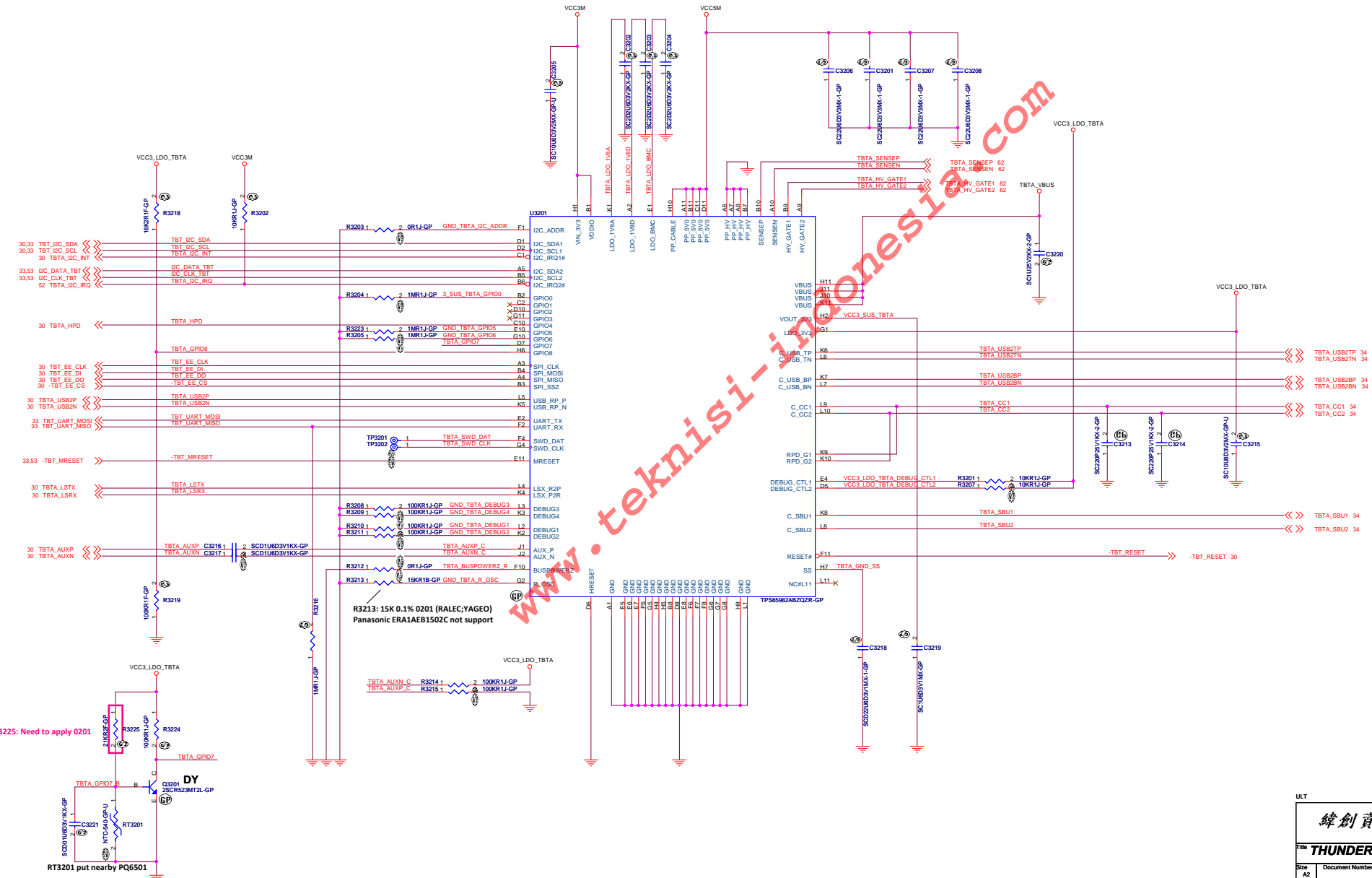
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
* ALPINERIDGE_SP(2/2)	
Document Number Raven-2	Rev SA
Date: Wednesday, April 27, 2016	Sheet 31 of 89


Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	1	DEBUG_CTL2	DEBUG_CTL1	I2C_ADDR			R/W

U3201	R3203	I2C_ADDR
Master 0	0	000b
Slave 1	93.1K	001b
Slave 2	156K	010b
Slave 3	220K	011b
Slave 4	280K	100b
Slave 5	340K	101b
Slave 6	402K	110b
Slave 7	Open	111b

```
20160408_RV2_SDV_EC171
' - correction of I2C address table
- change R3304 to DY
```

--



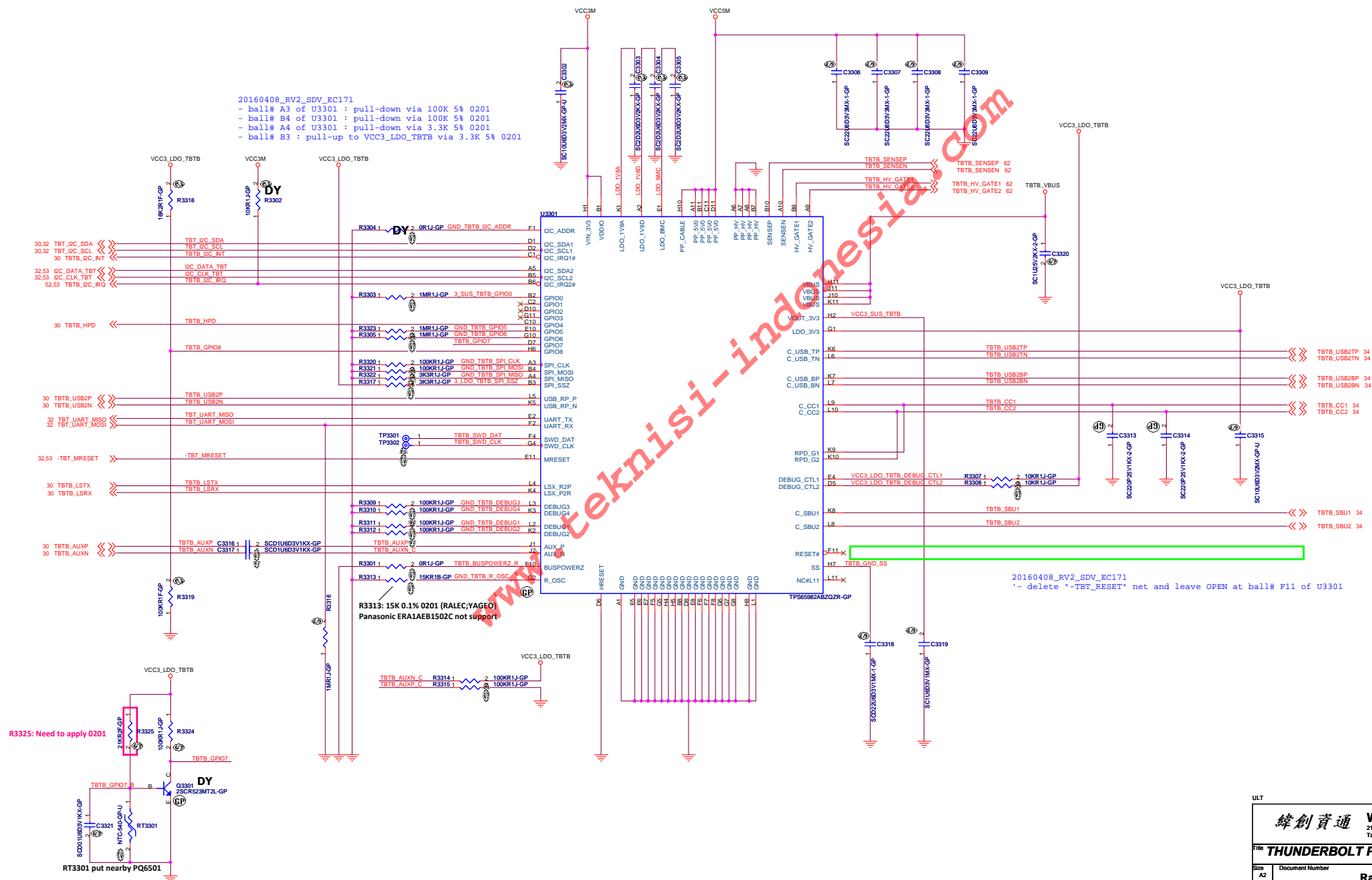
 緯創資通		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
THUNDERBOLT PORT Port-A			
# A2	Document Number Raven-2	Rev SA	
Date: Thursday, May 05, 2016		Sheet 32 of	89

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	1	DEBUG_CTL2	DEBUG_CTL1	I2C_ADDR			R/W

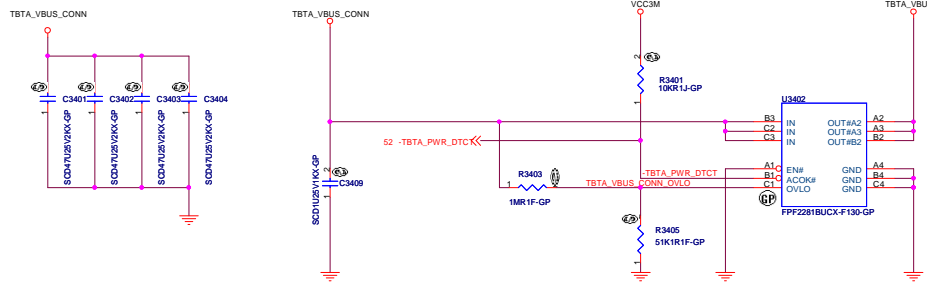
U3301	R3304	I2C_ADDR
Master 0	0	000b
Slave 1	93.1K	001b
Slave 2	156K	010b
Slave 3	220K	011b
Slave 4	280K	100b
Slave 5	340K	101b
Slave 6	402K	110b
Slave 7	Open	111b

← LOGIC

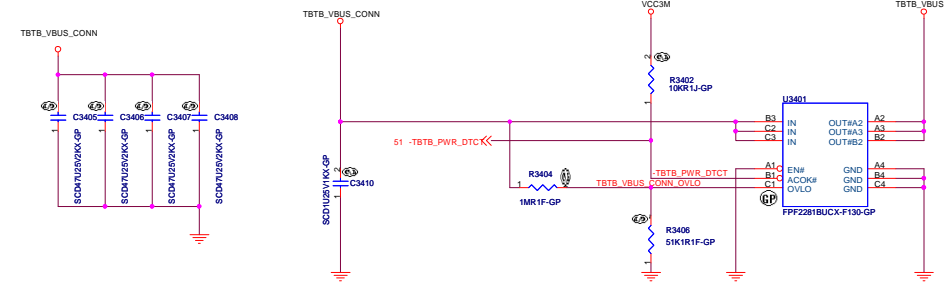
```
20160317_RV2_SDV_EC122
- add one more TI DP control circuit
- Ref Des (unit #) should be modified
- change net names from "TBTA_xx" to "TBTB_xx"
```



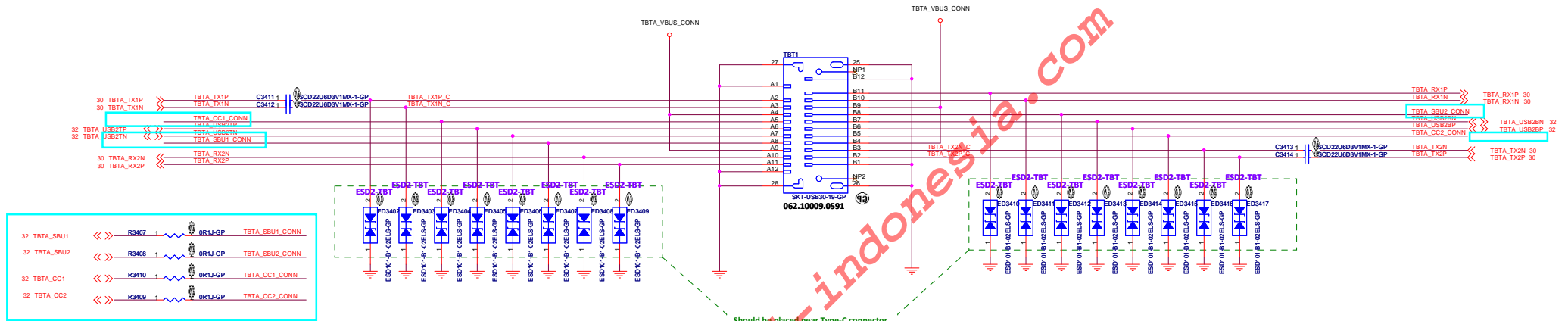
 緯創資通		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
THUNDERBOLT PORT B			
Size A2	Document Number	Raven-2	Rev SA
Date: Thursday, May 05, 2016		Sheet 33 of	89



Over Voltage Lock Out Trip Threshold = $1.20 * (1 + R3403 / R3405)$

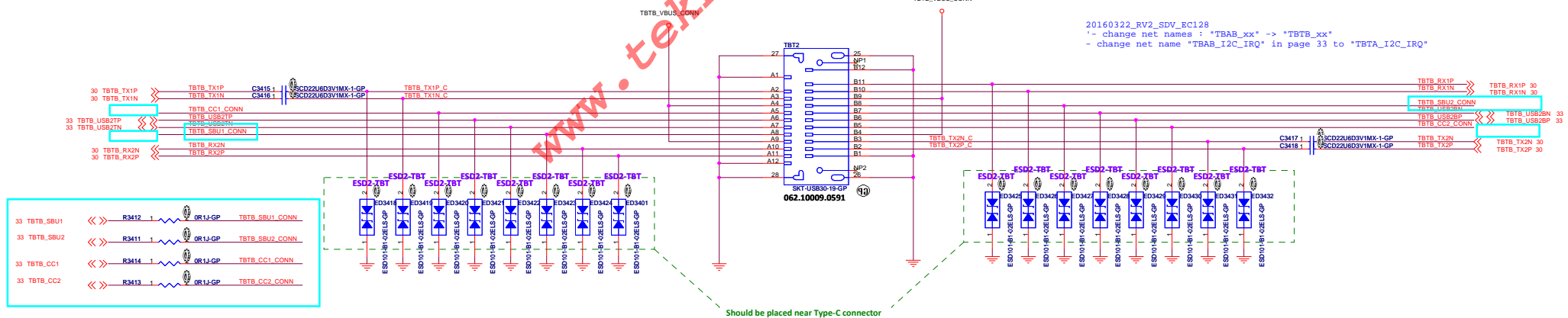


Over Voltage Lock Out Trip Threshold = $1.20 * (1 + R3404 / R3406)$



Should be placed near Type-C connector

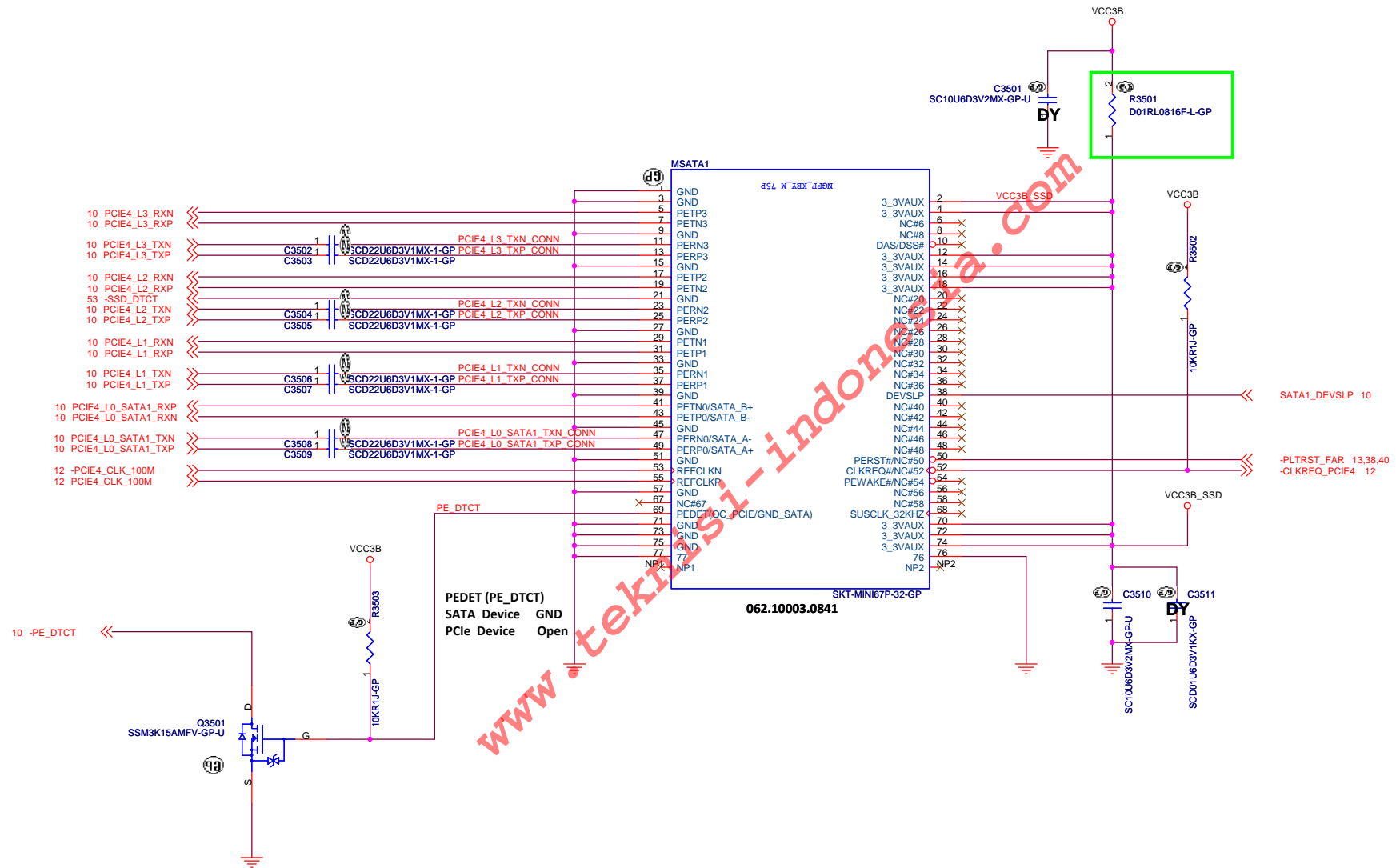
20160408_RV2_SDV_EC175
 - change net names in page34
 TBTx_SBUx -> TBTx_SBUx_CONN
 - delete off-page connection
 TBTx_CCx_CONN, TBTx_SBUx
 - add 60hm jumpers (total 6x) between TBTx_SBUx and TBTx_SBUx_CONN and between TBTx_CCx and TBTx_CCx_CONN



Should be placed near Type-C connector

20160322_RV2_SDV_EC128
 '- change net names : "TBAB_xx" -> "TBTB_xx"
 - change net name "TBAB_I2C_IRQ" in page 33 to "TBTB_I2C_IRQ"

20160406_RV2_SDV_EC159
'- delete R3501
- add D01RL0816F-L between VCC3B and VCC3B_SSD



ULT

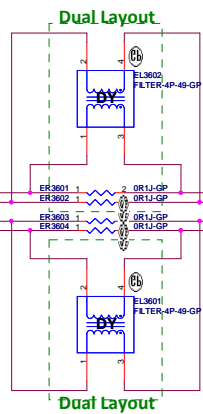
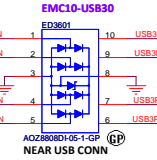
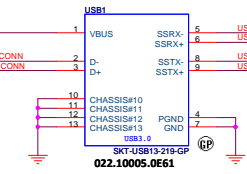
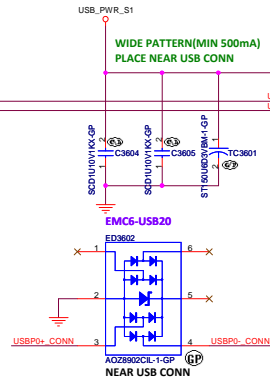
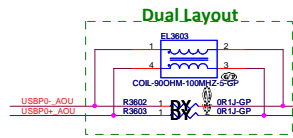


TABLE of TVS DIODE: D3601,D3604

	Vendor	Vendor P/N	Wistron P/N
1st	AOS	AOZ8808DI-05	75.08808.073
2nd	SEMTECH	RClamp0524PATCT	75.00524.073
3rd			

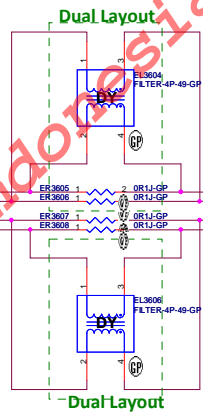
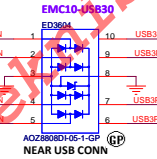
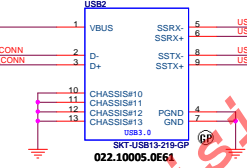
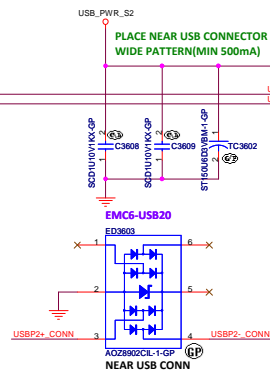
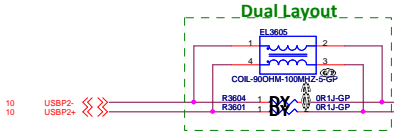
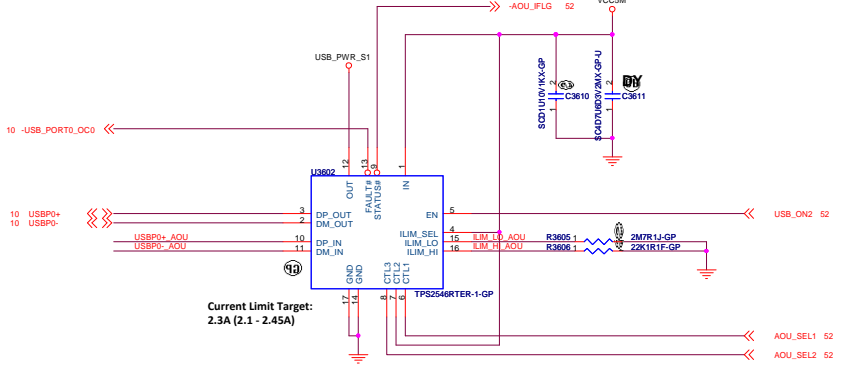
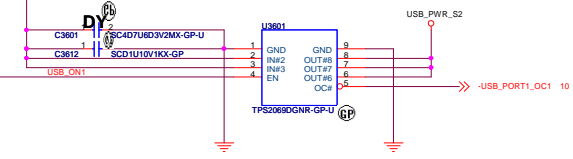
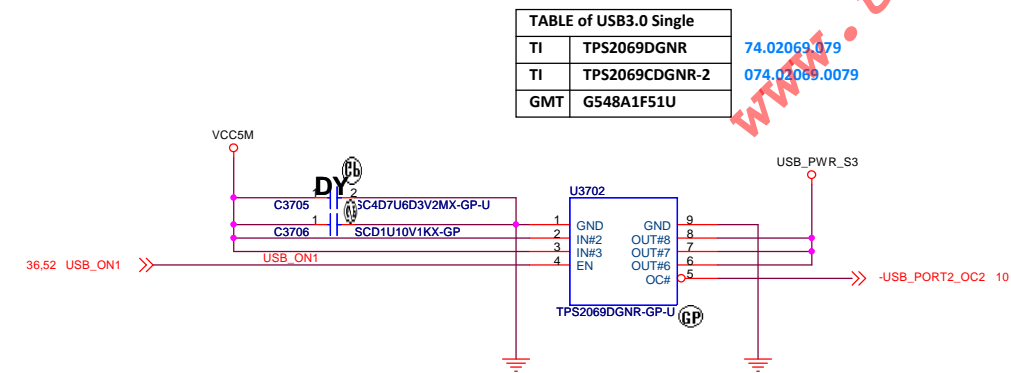
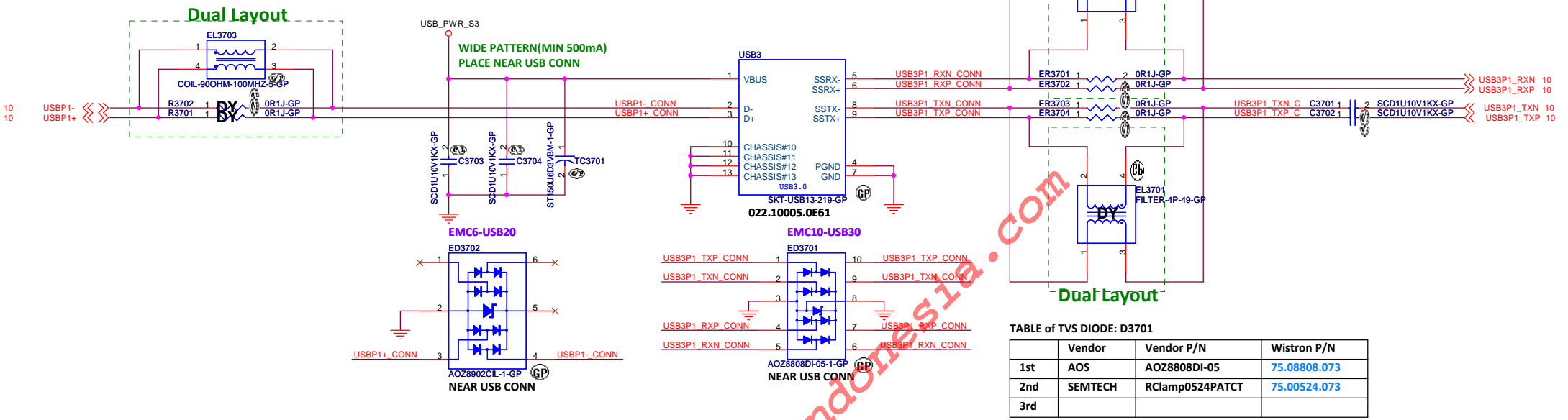


TABLE of USB3.0 Single

T1	TP52069DGNR	74.02069.079
T1	TP52069CDGMR-2	074.02069.079
GMT	G548A1F51U	



Current Limit Target:
2.3A (2.1 - 2.45A)



20160406_RV2_SDV_EC163

'- change connection of ball# L4 of U3001 to "-PLTRST_NEAR"
- change connection of pin# 36 of U3801 to "-PLTRST_FAR"

TABLE

vPro Capability		
GbE PHY	Yes	No
U3801	Jacksonville-LM	Jacksonville-V

LOGIC

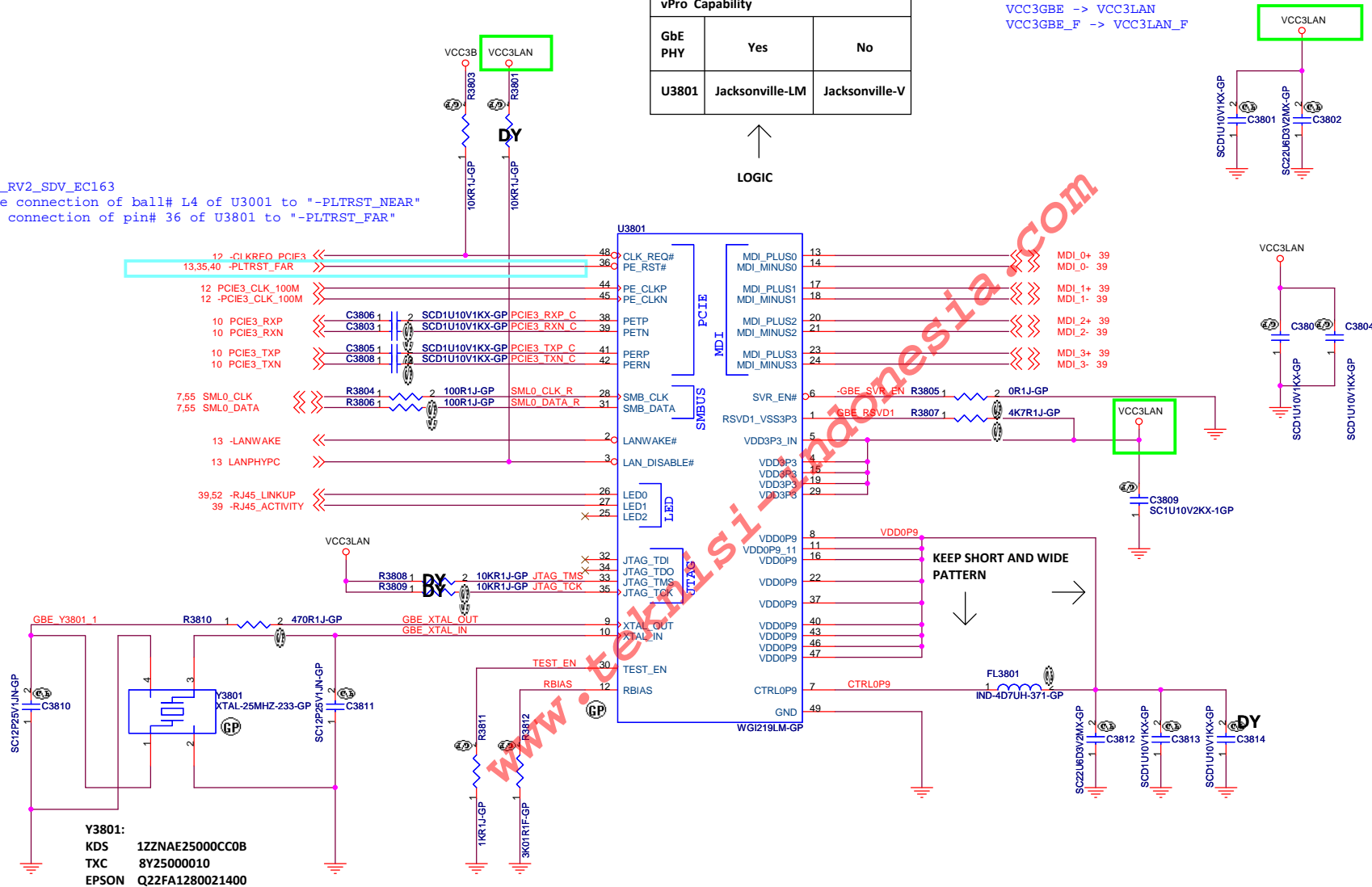
20160406_RV2_SDV_EC158

'- delete R3802

- change net names :

VCC3GBE -> VCC3LAN

VCC3GBE_F -> VCC3LAN_F

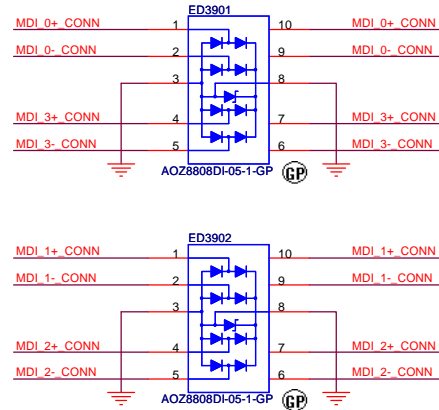
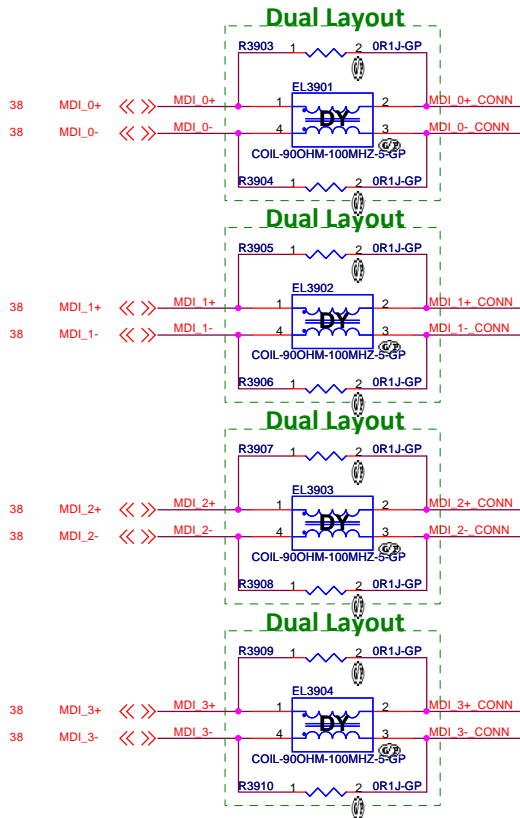


ULT

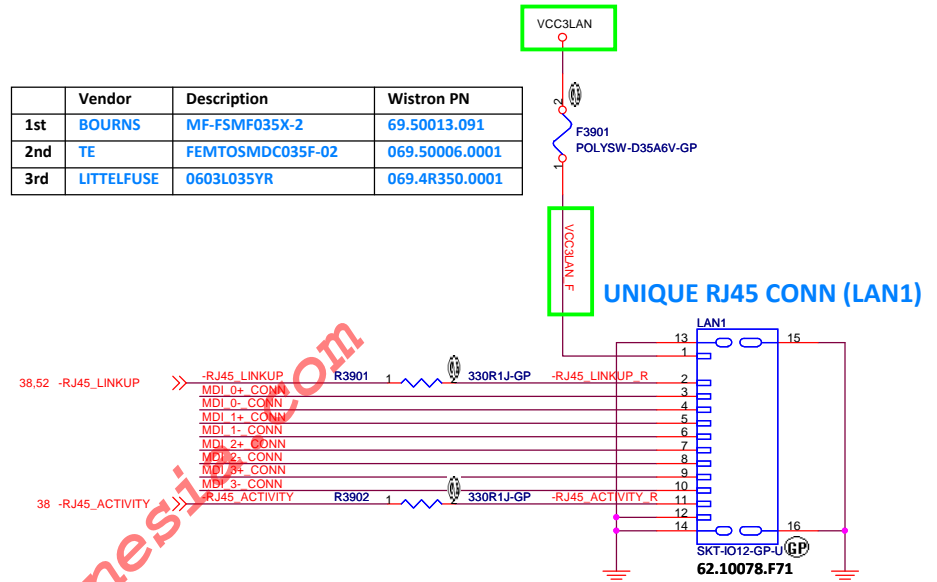
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title **GBE JACKSONVILLE**

Size A3	Document Number	Rev SA
Date: Thursday, May 05, 2016	Raven-2	89



	Vendor	Description	Wistron PN
1st	BOURNS	MF-FSMF035X-2	69.50013.091
2nd	TE	FEMTOSMDC035F-02	069.50006.0001
3rd	LITTELFUSE	0603L035YR	069.4R350.0001



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ULT

2630S3 CONNECTOR



Size A3	Document Number Raven-2	Rev SA
Date: Thursday, May 05, 2016	Sheet 40 of 89	

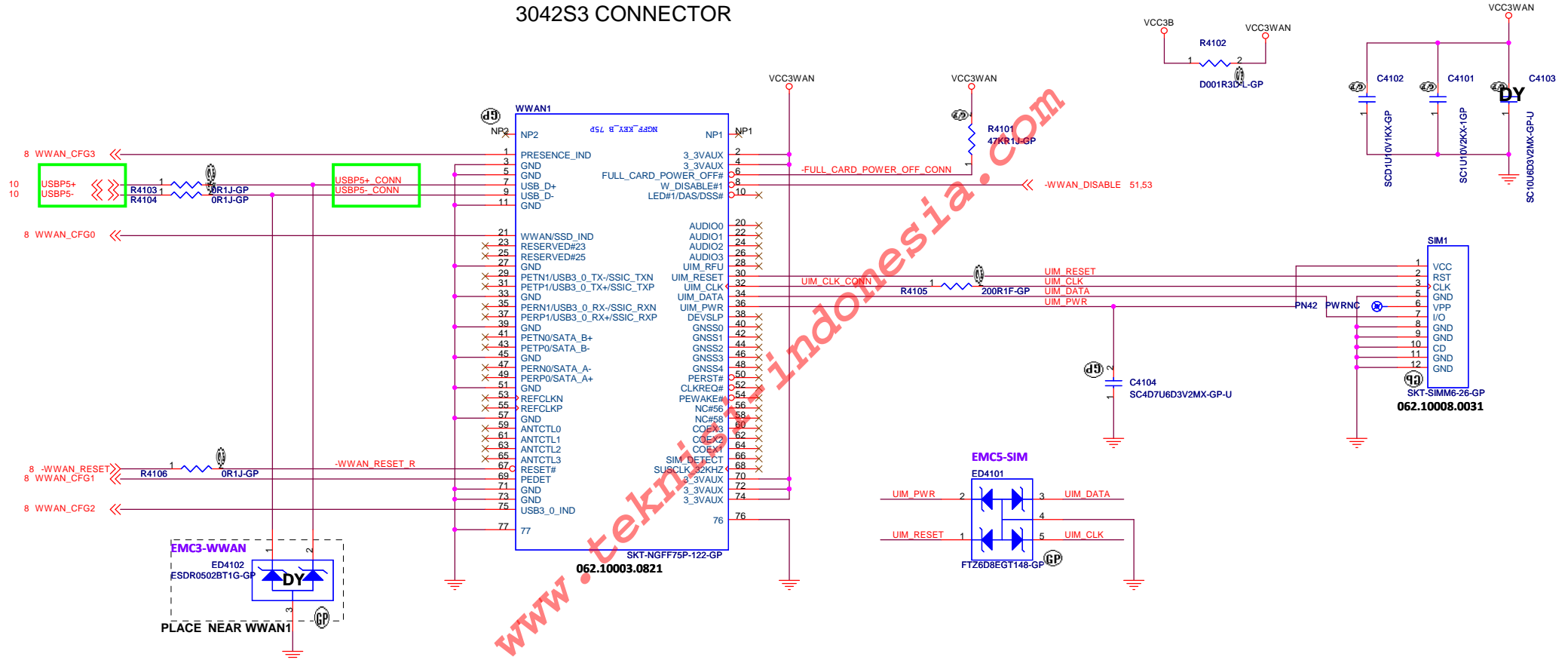

```

20160331_RV2_SDV_EC155
'- net "USBP1-" connects to pin# 1 of L3703
- net "USBP1+" connects to pin#2 of L3703
- change net names "USBP5-_CONN" and "USBP5+_CONN" in page 37 to "USBP1-_CONN" and "USBP1+_CONN".
- net "USBP5+" connects to pin#1 of R4103
- net "USBP5-" connects to pin#1 of R4104
- change net names "USBP1-_CONN" and "USBP1+_CONN" in page 41 to "USBP5-_CONN" and "USBP5+_CONN".

```

TYPE-B M.2 CARD FOR WWAN

3042S3 CONNECTOR



ULT

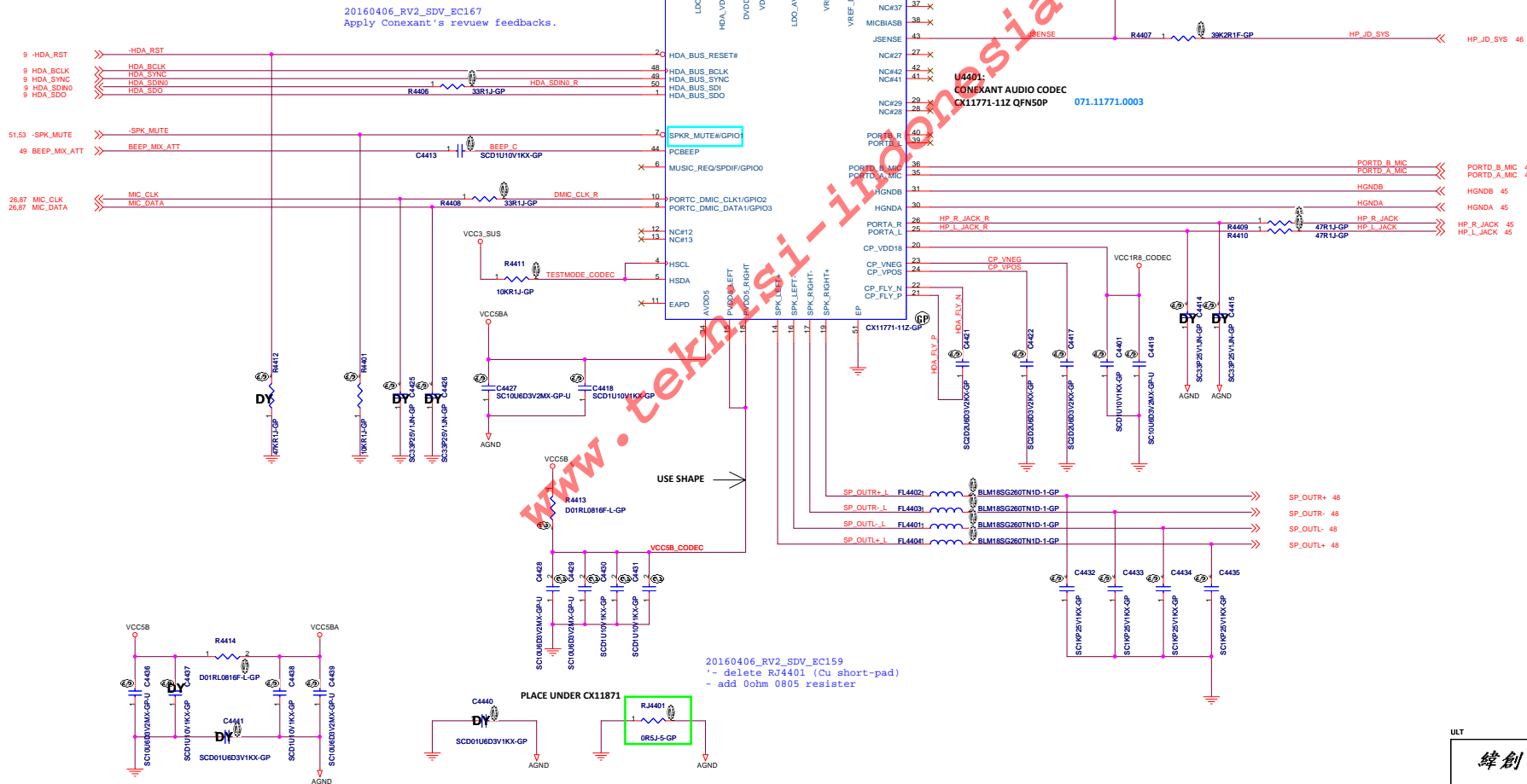
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title **PCIE M.2 CARD SLOT 2**

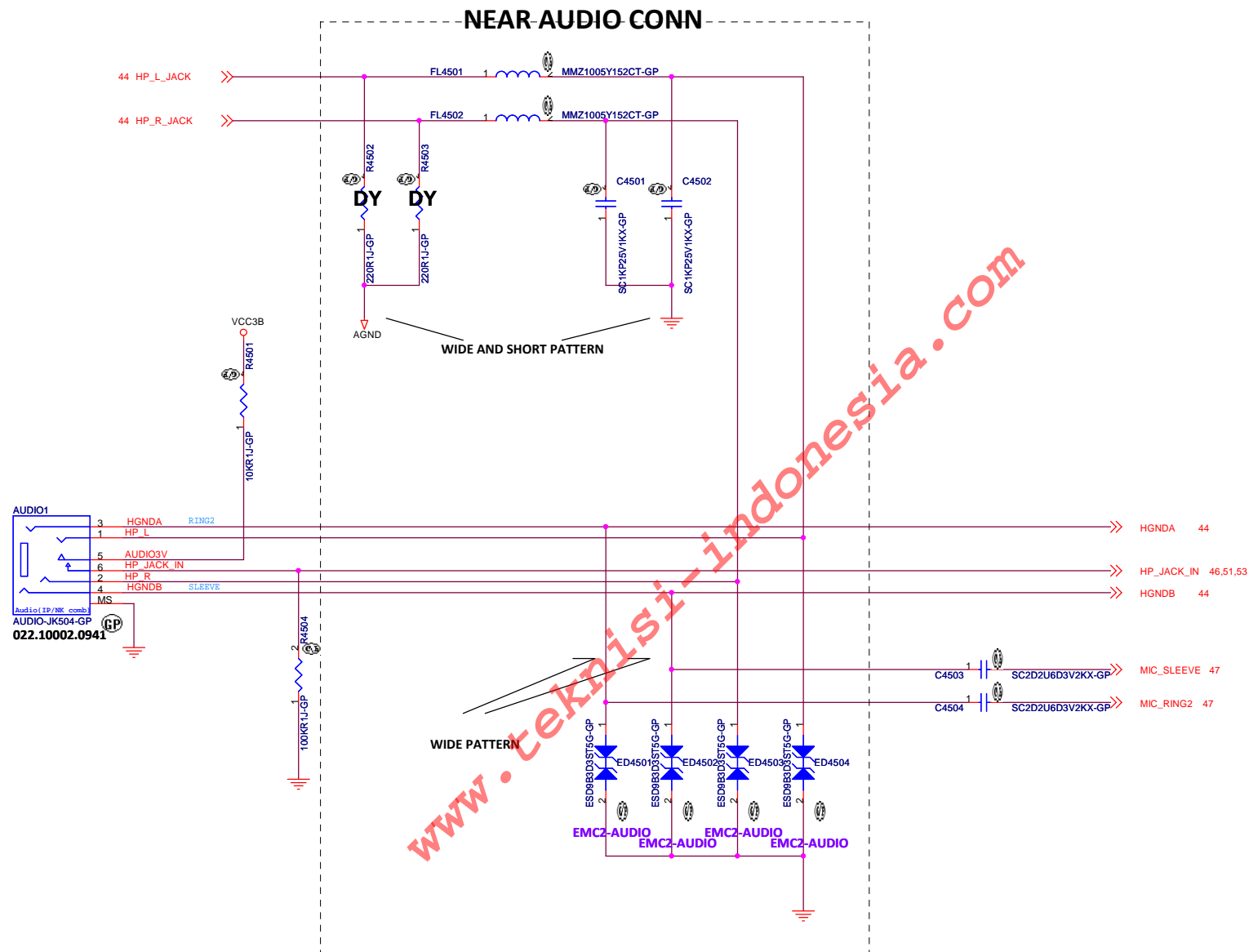
Size A3	Document Number Raven-2	Rev SA
Date: Thursday, May 05, 2016	Sheet 41 of 89	

TABLE MIC HW ENABLE/DISABLE		
	ENABLE	DISABLE
R823	ASM	NO ASM
R4408	ASM	NO ASM

The diagram shows the wiring for the NEAR Audio Codec U4401. It includes two resistors, R4415 and R4416, both labeled as 10K. R4415 connects VCC3B to the MIC_VCC pin. R4416 connects GND to the MIC_GND pin. The components are labeled with their respective pin numbers (1 and 2) and the component name (OR402-PAD-1-GP).



ULT			
緯創資通		Wistron Corporation 21F, 88, Sec. 5, Hsin Tai Wu Rd., Hsichuh, Taipei Hsien 221, Taiwan, R.O.C.	
Title AUDIO CX11771-11Z			
Size A2	Document Number	Raven-2	Rev SA
Date: Thursday, May 05, 2016		Sheet 44 of 89	



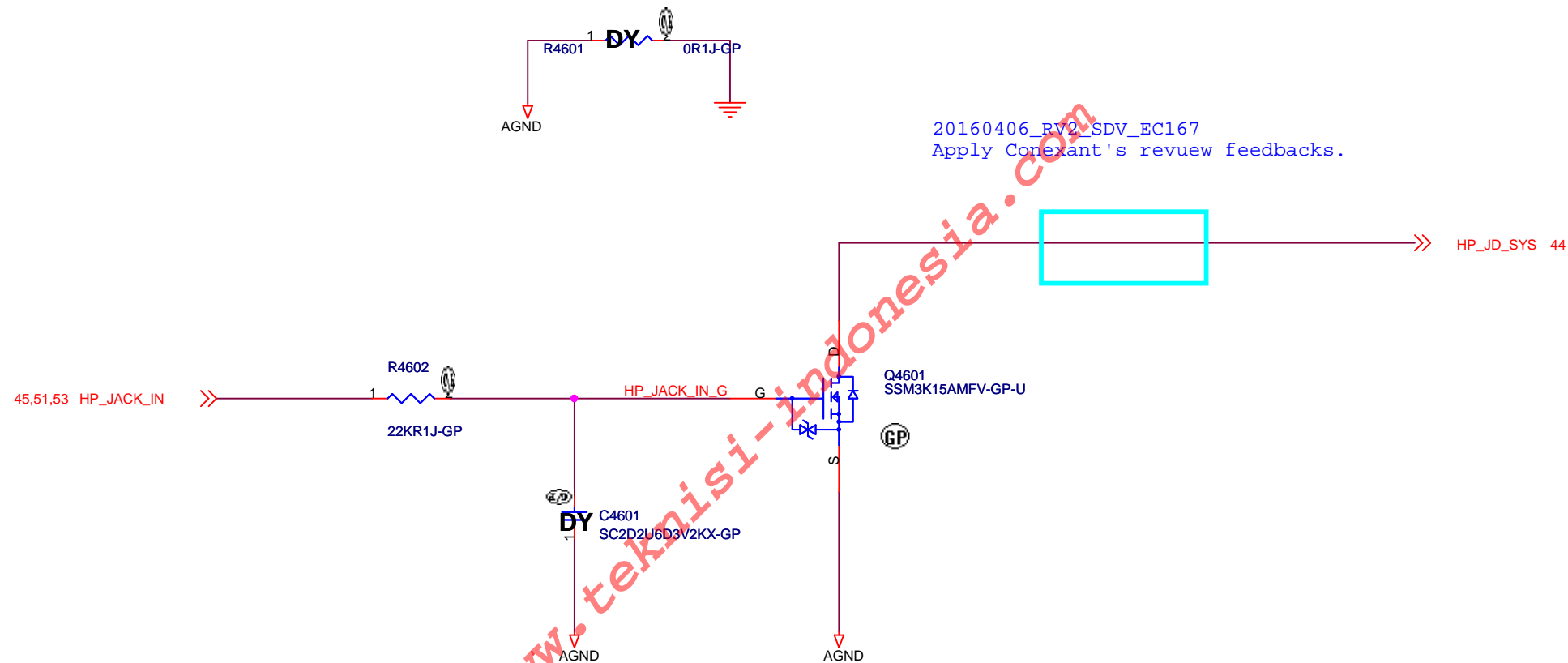
ULT

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title **AUDIO CONNECTOR**

Size A3 Document Number **Raven-2** Rev SA

Date: Thursday, May 05, 2016 Sheet 45 of 89



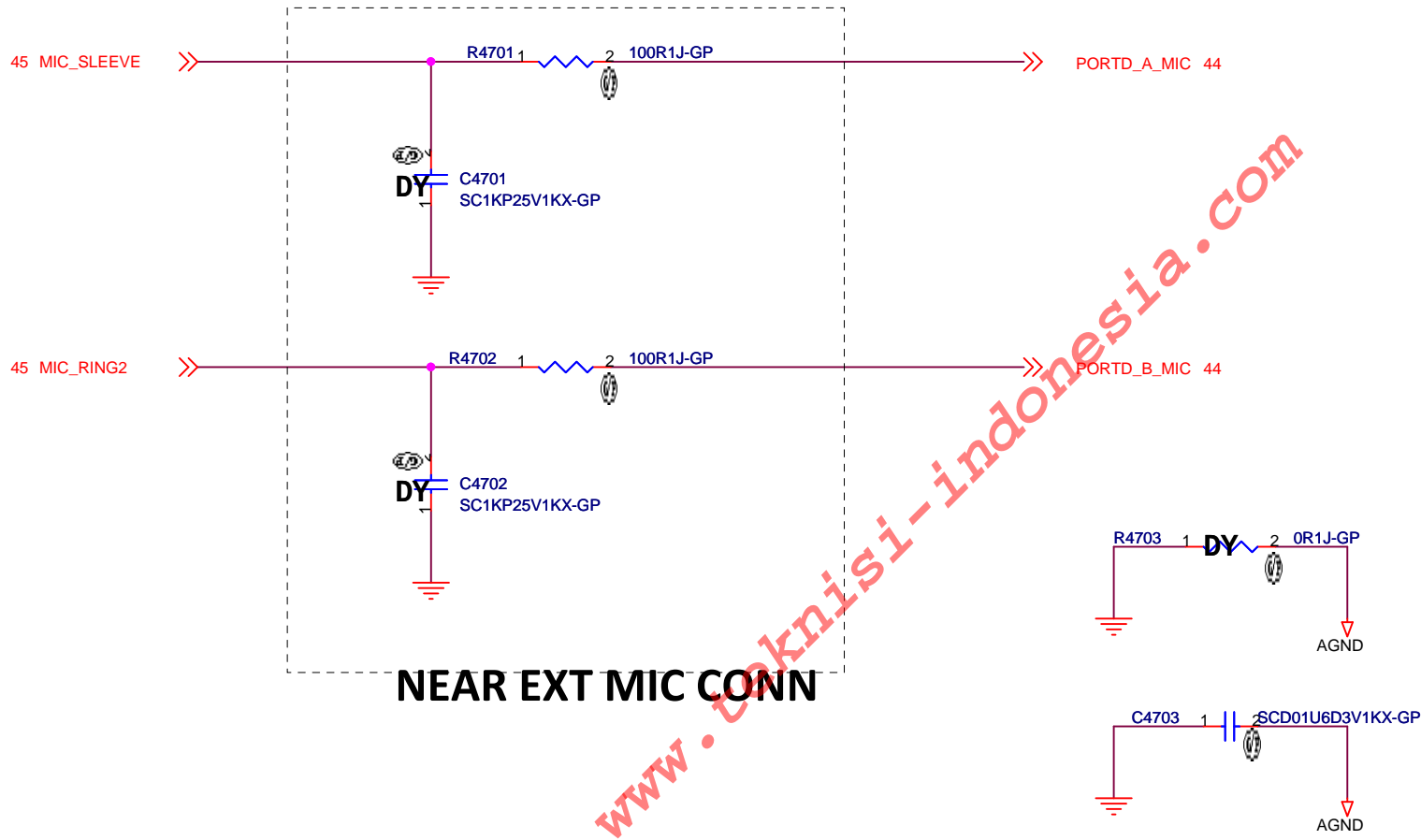
ULT

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title **AUDIO JACK SENSE**

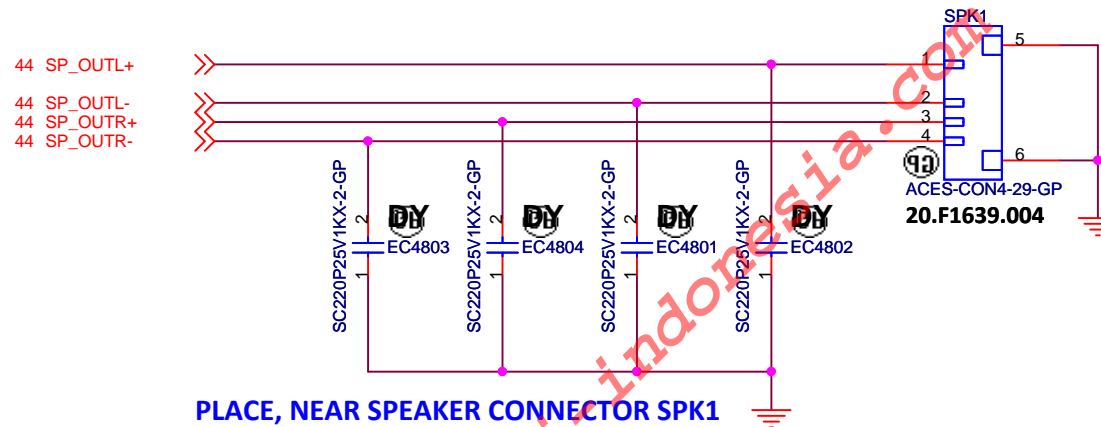
Size A4	Document Number Raven-2	Rev SA
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Date: Thursday, May 05, 2016	Sheet 46 of 89
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ULT

<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>	
Title AUDIO EXT MIC I/F	
Size A4	<div>Document Number</div> <div>Raven-2</div>
	<div>Rev</div> <div>SA</div>
Date: Thursday, May 05, 2016	Sheet 47 of 89

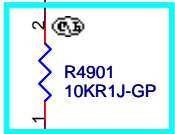


ULT

緯創資通		Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title AUDIO SPEAKER			
Size A4	Document Number Raven-2		Rev SA
Date: Thursday, May 05, 2016		Sheet 48 of	89

9 PCH_SPKR

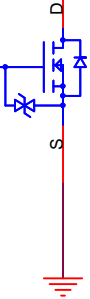
20160406_RV2_SDV_EC167
Apply Conexant's revuew feedbacks.



BEEP_MIX_ATT 44

51,53 -BEEP_ENABLE

G



Q4901
SSM3K15AMFV-GP-U

ULT

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title **AUDIO BEEP**

Size
A4

Document Number

Raven-2

Rev
SA

Date: Thursday, May 05, 2016

Sheet 49 of 89

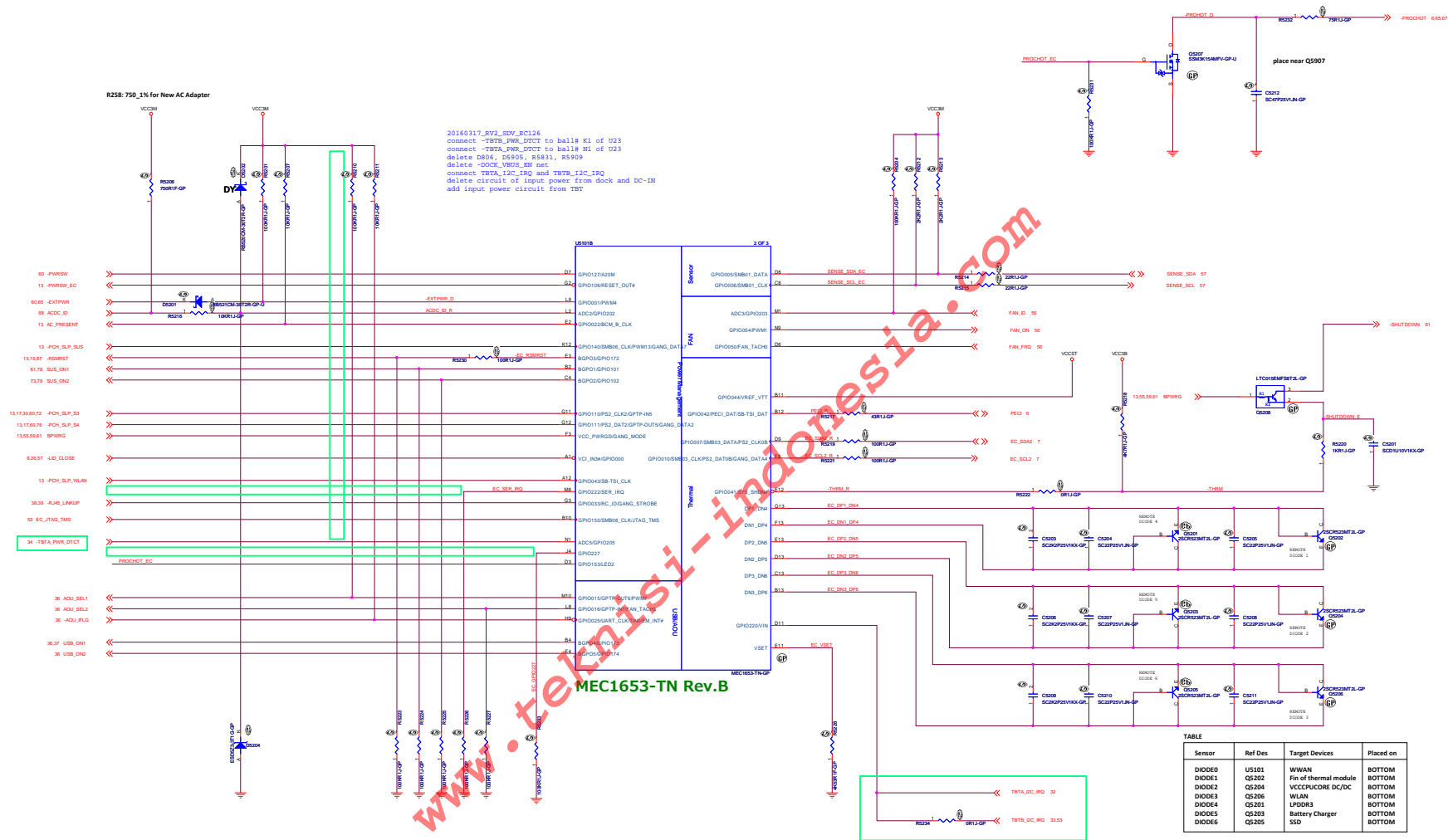
20160317_RV2_SDV_EC120
Delete all circuit in page 50

BLANK

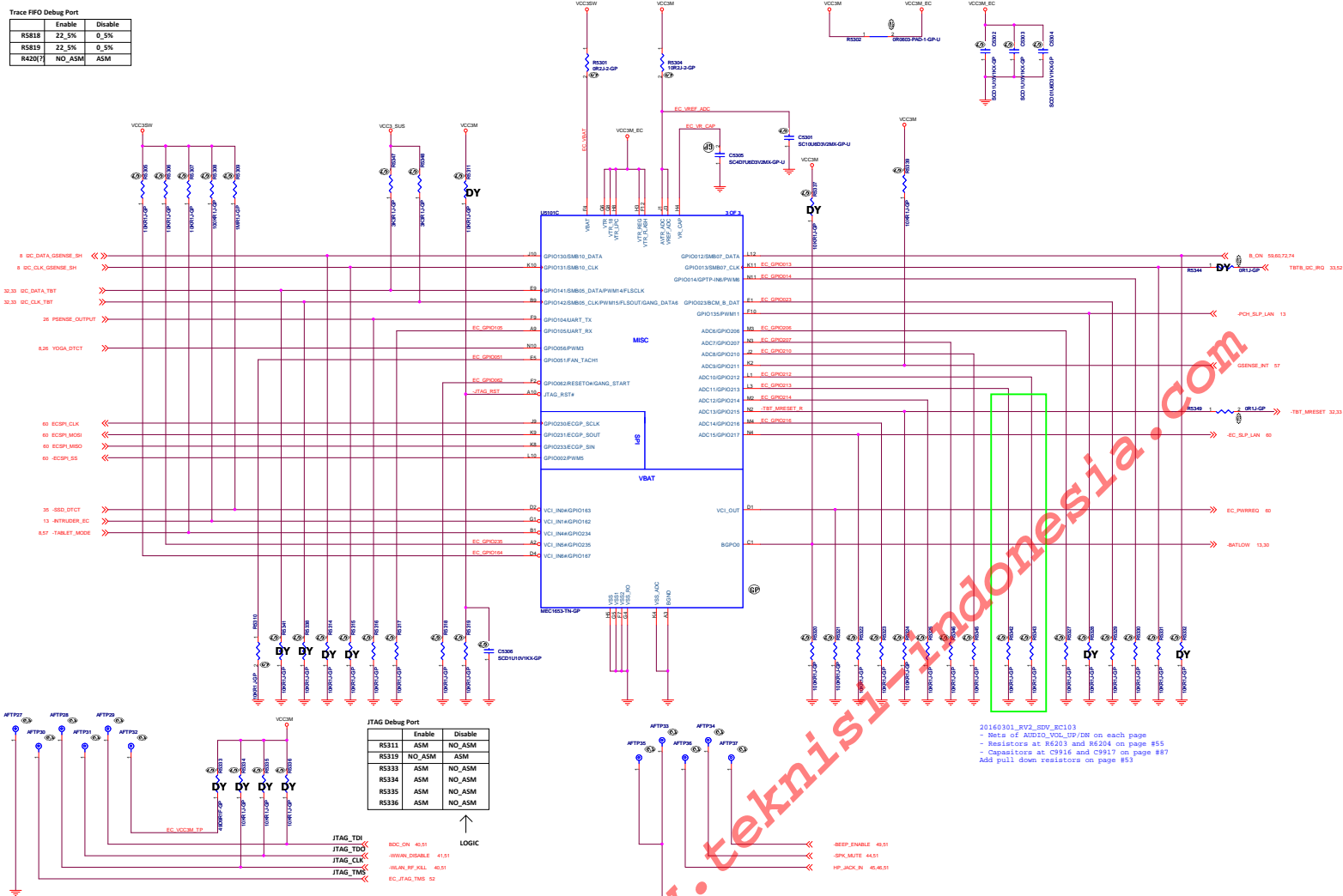
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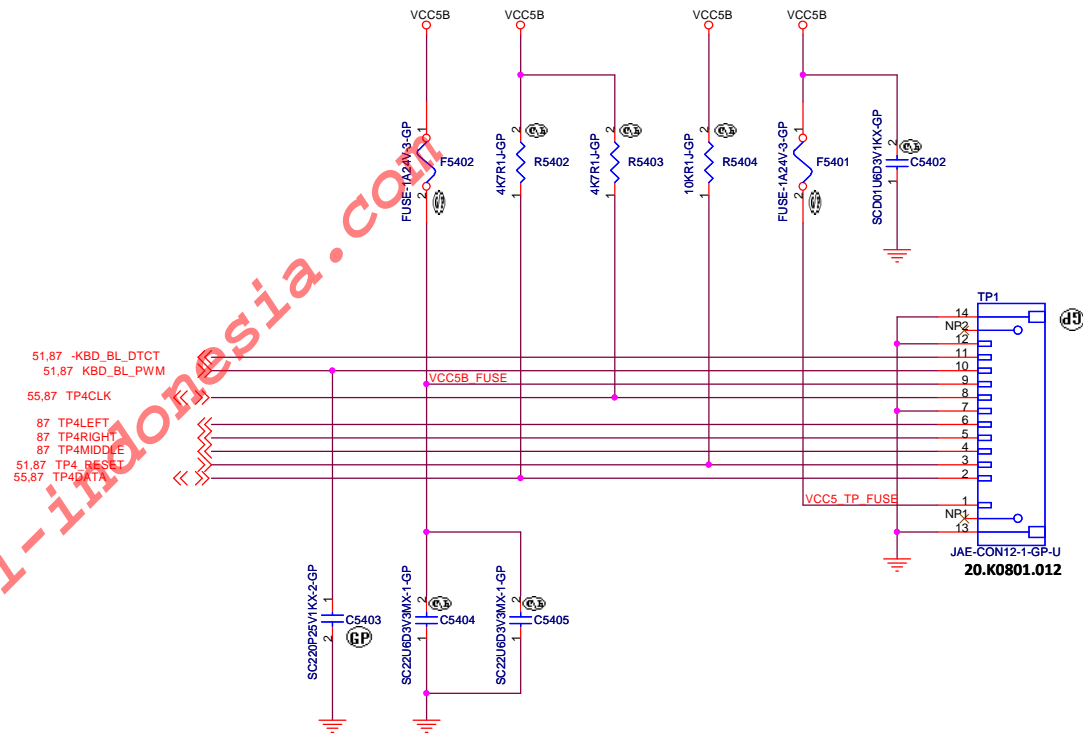
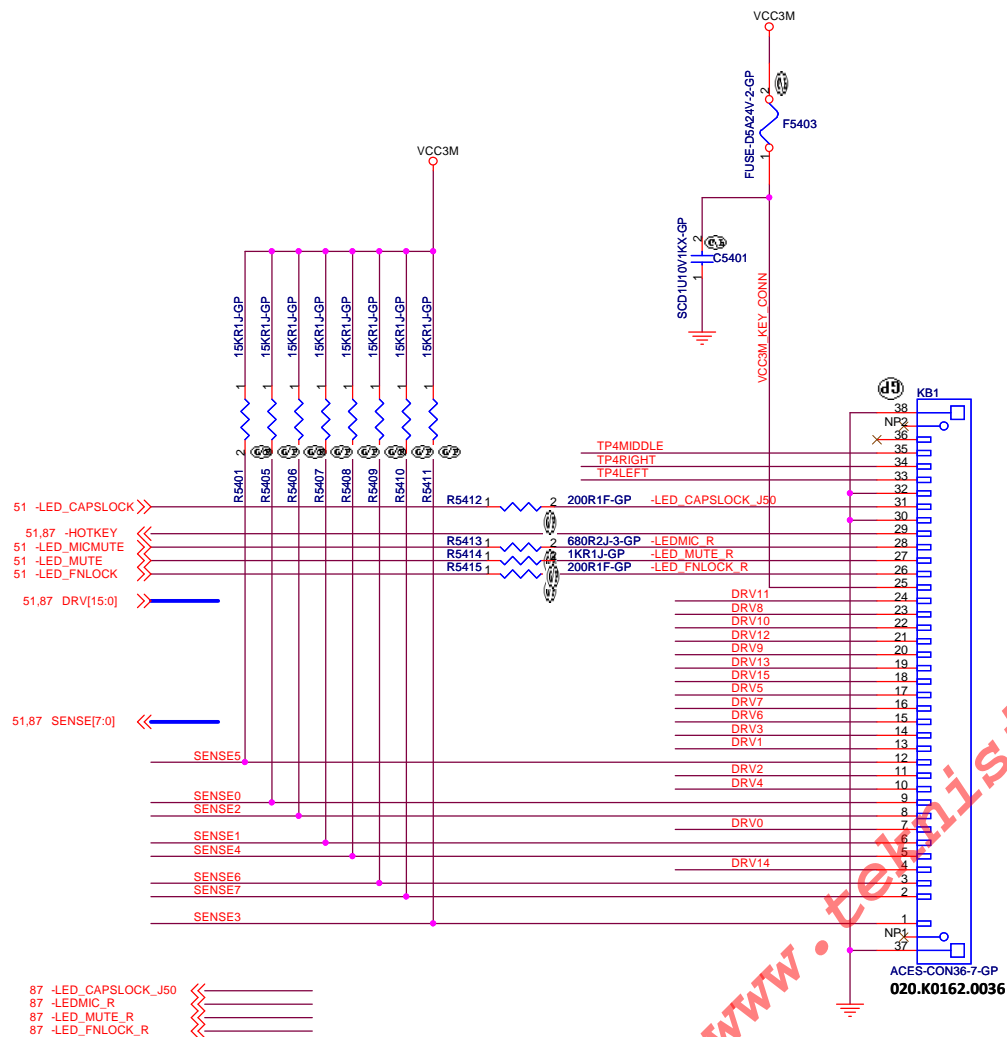
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緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title BLANK			
Size A4	Document Number Raven-2		Rev SA
Date: Wednesday, April 27, 2016		Sheet 50 of	89

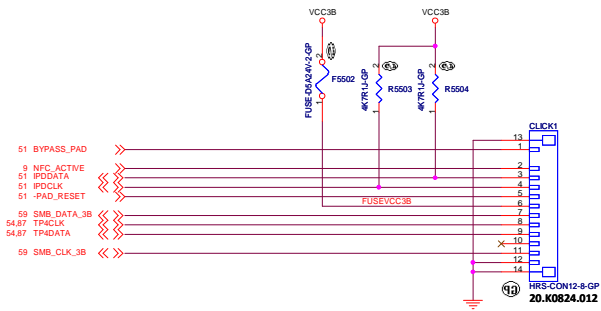


	Enable	Disable
R5818	22_5%	0_5%
R5819	22_5%	0_5%
R420[7]	NO_ASM	ASM

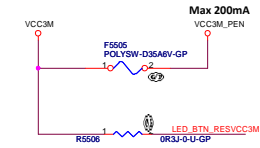




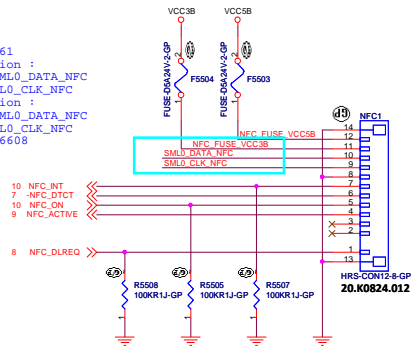
ULT



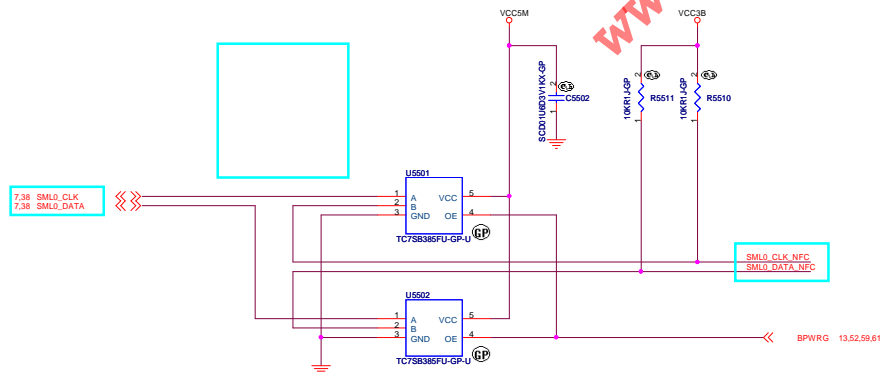
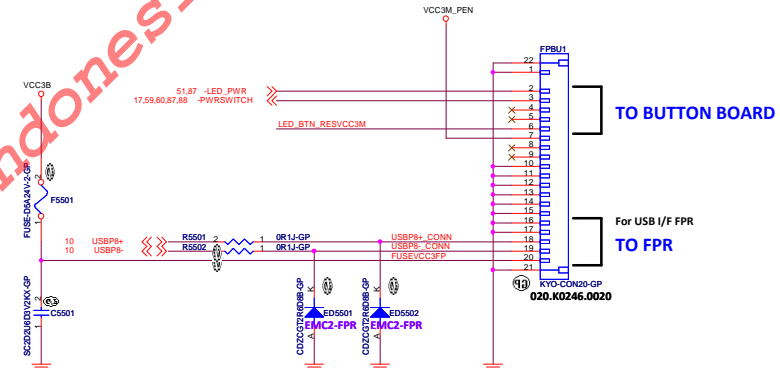
TO SUB BOARD

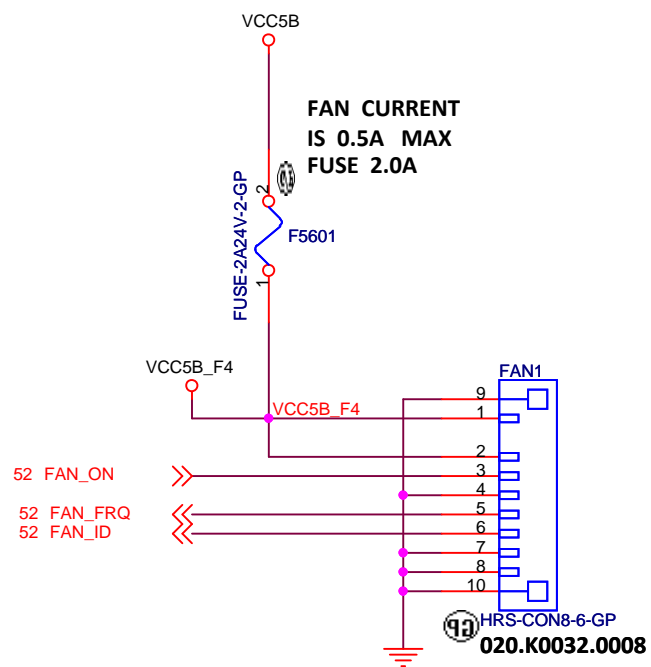


20160406_RV2_SDV_EC161
 - change net connection :
 pin#10 of NFC1 : SML0_DATA_NFC
 pin#9 of NFC1 : SML0_CLK_NFC
 - change net connection :
 pin#10 of NFC1 : SML0_DATA_NFC
 pin#9 of NFC1 : SML0_CLK_NFC
 - delete R6605 and R6608



20160301_RV2_SDV_EC103
 - Nets of AUDIO1_VOL_UP/DN on each page
 - Resistors at R6203 and R6204 on page #55
 - Capacitors at C9916 and C9917 on page #87
 Add pull down resistors on page #53



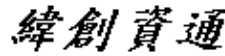


PIN# NET NAME

- PIN1 VCC5B_F4
- PIN2 (OPEN)
- PIN3 FAN_ON
- PIN4 GND
- PIN5 FAN_FRQ
- PIN6 FAN_ID
- PIN7 GND
- PIN8 GND

FAN ID		Inside of Thermal Module
HIGH	Secondary Source	Open
LOW	Primary Source	Tie down to GND

ULT

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title FAN CONNECTOR			
Size A4	Document Number Raven-2		Rev SA
Date: Thursday, May 05, 2016		Sheet 56 of 89	

Accel for EC

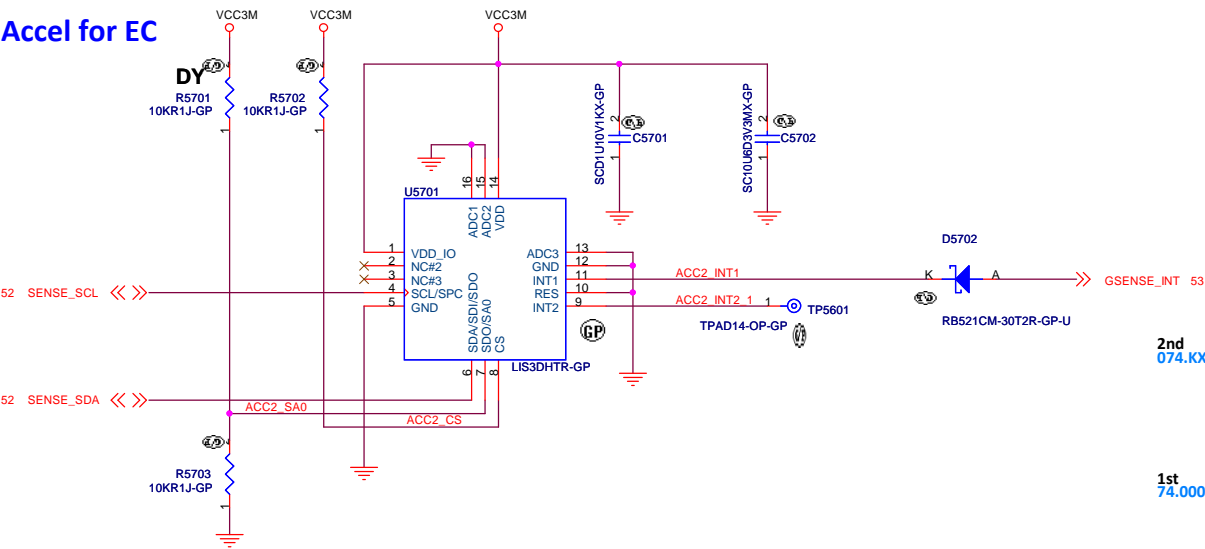


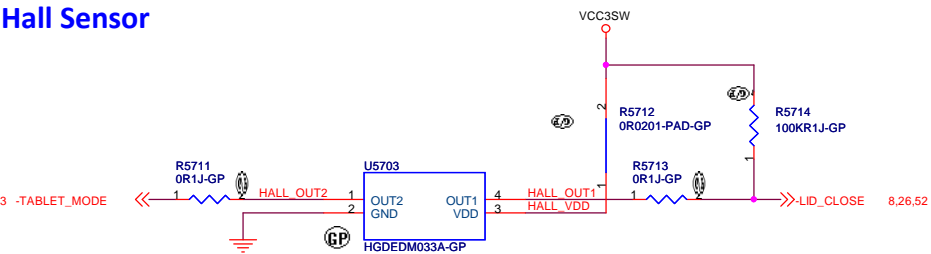
TABLE	
CS	Mode Selection
H	I2C Mode
L	SPI Mode

← Logic

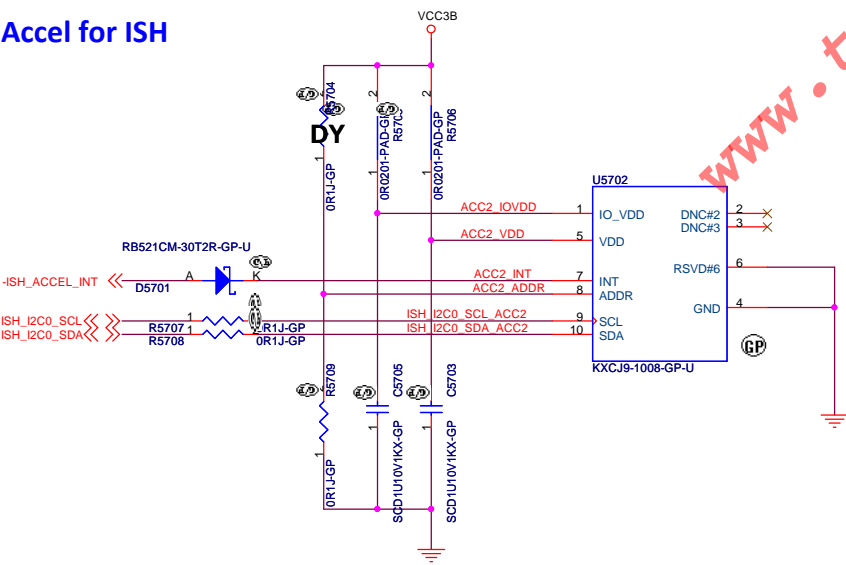
TABLE		
Sensor IC	ACC2_SA0	I2C Address
Kionix KX023-1025	H	3Eh (Write) 3Fh (Read)
	L	3Ch (Write) 3Dh (Read)
ST Micro LIS3DSH	H	3Ah (Write) 3Bh (Read)
	L	3Ch (Write) 3Dh (Read)

← Logic

Hall Sensor



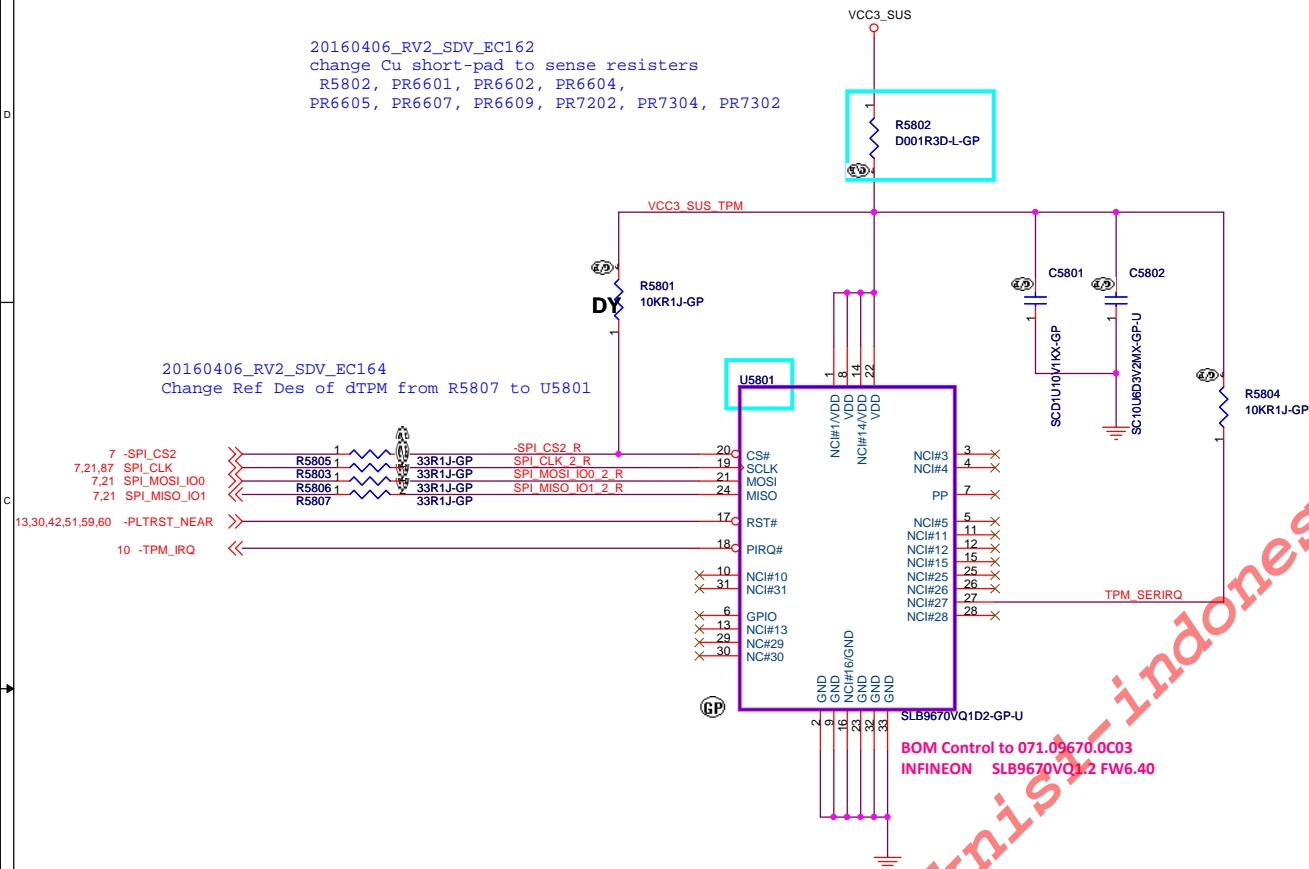
Accel for ISH



20160406_RV2_SDV_EC162
change Cu short-pad to sense resistors
R5802, PR6601, PR6602, PR6604,
PR6605, PR6607, PR6609, PR7202, PR7304, PR7302

20160215_RV2_SDV_EC082
update ST Micro dTPM component

TABLE				
Pin No	TCG PTP Spec (v38)	Infineon SLB9670VQ1.2 FW 6.40	ST Micro ST33HTPH2E32AAE5	Nuvoton TBD
1	VDD	VDD	NC	VSB
2	GND	GND	GND	NC
3	GPIO	NC	NC	GPX/GPIO2
4	GPIO	NC	PP	PP
5	NC	NC	NC	TEST
6	VNC/GPIO	GPIO	NC	GPIO3
7	GPIO/VDD	PP	GPIO	NC
8	VDD	VDD	NC	VDD
9	GND	GND	NC	GND
10	VNC/GPIO	NC	NC	NC
11	NC	NC	NC	NC
12	NC	NC	NC	Reserved
13	VNC/GPIO	NC	NC	GPIO4
14	VDD	NC	NC	VDD
15	NC	NC	NC	DNC
16	GND	NC	NC	GND
17	SPI_RST#	RST#	SPI_RST#	SPI_RST#
18	SPI_PIRQ#	PIRQ#	SPI_PIRQ#	SPI_IRQ#
19	SPI_CLK	SCLK	SPI_CLK	SCLK
20	SPI_CS#	CS#	SPI_CS#	SCS#
21	MOSI	MOSI	MOSI	MOSI
22	VDD	VDD	VPS	VDD
23	GND	GND	NC	GND
24	MISO	MISO	MISO	MISO
25	NC	NC	NC	NC
26	NC	NC	NC	NC
27	NC	NC	NC	(SERIRQ)
28	NC	NC	NC	DNC
29	VNC/GPIO	NC	NC	GPIO0
30	VNC/GPIO	NC	NC	GPIO1
31	VNC	NC	NC	NC
32	GND	GND	NC	GND



ULT

TABLE

REF DES	ENABLE	DISABLE
LPC1	ASM	NO_ASM
R710	ASM	NO_ASM

LOGIC

DY

LPC1

7,87 LPCCLK_DEBUG_24M
7,51 -LPC_FRAME
7,51 -CLKRUN
7,51 IRQSER
13,30,42,51,58,60 -PLTRST_NEAR
53,60,72,74 B_ON

ACES-CONN14D-2-GP-U
20.F1856.014
(ASM: SDV only)

-PWRSWITCH 17,55,60,87,88
LPC_AD0
LPC_AD1
LPC_AD2
LPC_AD3

-SUS_STAT 7,51

LPC_AD[3:0] 7,51

LPC for Debug Card Connector

7,51 LPC_AD[3:0]

VCC3M

DY

LPC2

LPC_AD0
LPC_AD1
LPC_AD2
LPC_AD3

7,51 -LPC_FRAME
13,30,42,51,58,60 -PLTRST_NEAR
7,87 LPCCLK_DEBUG_24M

MLX-CONN10-7-GP
20.D0183.110
(ASM: SDV only)

55 SMB_CLK_3B
55 SMB_DATA_3B

U5901
TC7SB385FU-GP-U

U5902
TC7SB385FU-GP-U

SMB_CLK 7
SMB_DATA 7

BPWRG 13,52,55,61

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Title **SMBUS SWITCH/LPC DEBUG PORT**

Size A3 Document Number **Raven-2** Rev SA
Date: Thursday, May 05, 2016 Sheet 59 of 89

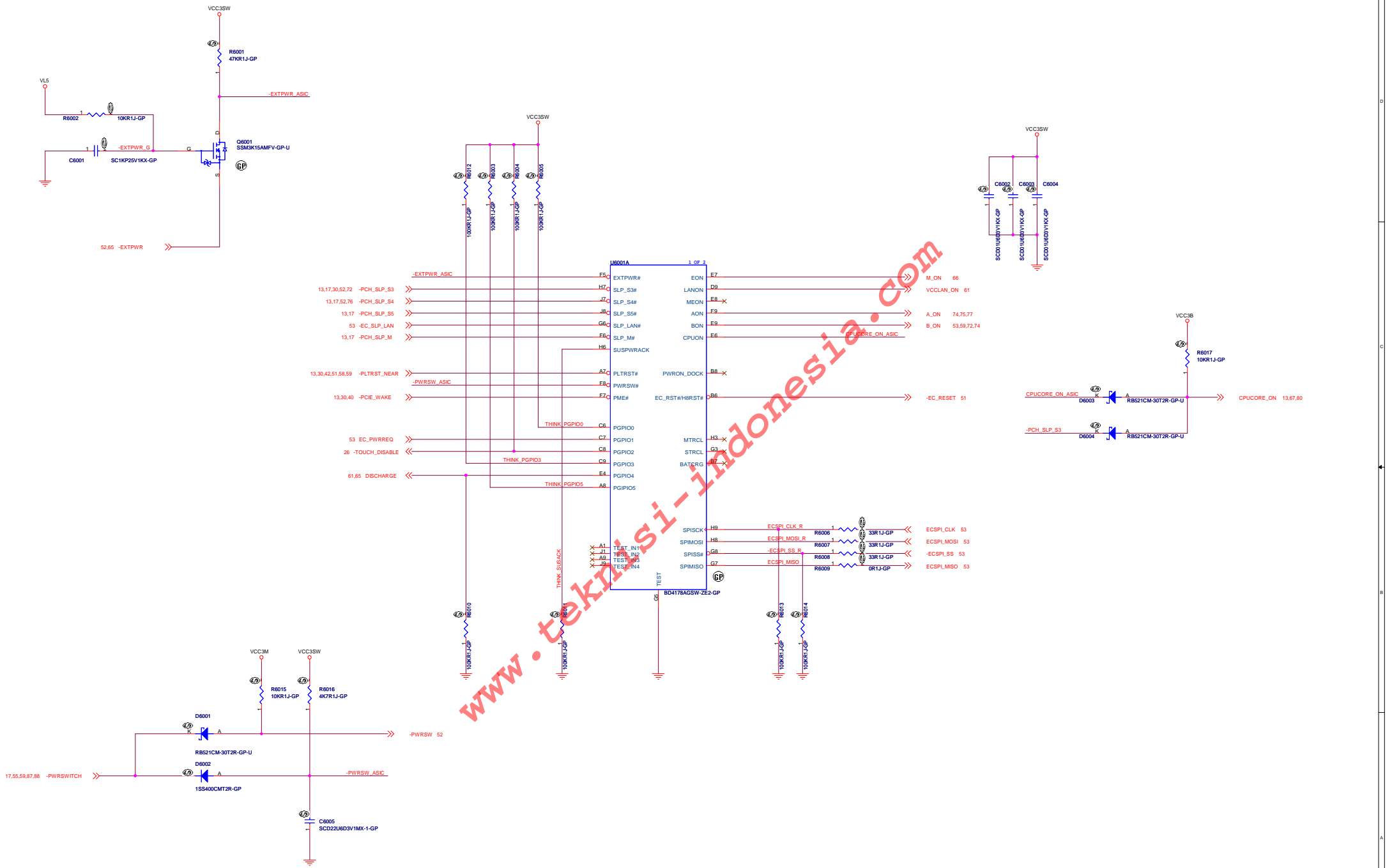
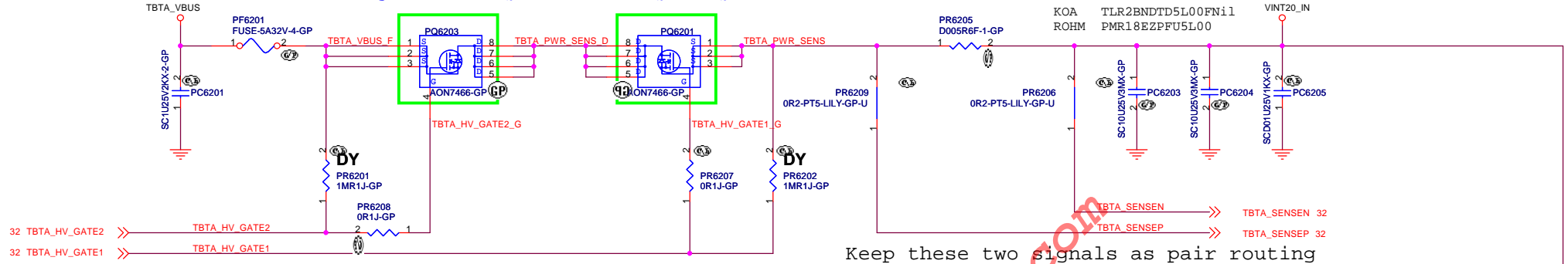
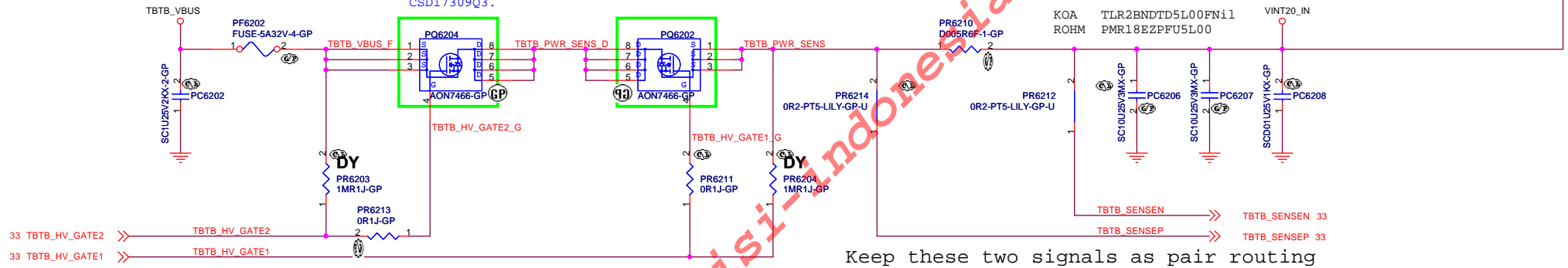


Table
PQ6201,PQ6202,PQ6203,PQ6204
1st AON7466 AOS
2nd SIS406DN VISHAY

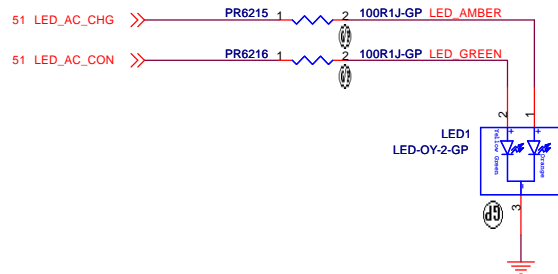
20160408_RV2_SDV_EC177
Change from CSD17309Q3 to AON7466 for PQ6201- PQ6204.



20160323_RV2_SDV_EC145
Change Q3716 and Q3703 from CSD16323Q3 to CSD17309Q3.



20160317_RV2_SDV_EC126
connect -TBTB_PWR_DTCT to ball# K1 of U23
connect -TBTA_PWR_DTCT to ball# N1 of U23
delete D806, D5905, R5831, R5909
delete -DOCK_VBUS_EN net
connect TBTA_I2C_IRQ and TBTB_I2C_IRQ
delete circuit of input power from dock and DC-IN
add input power circuit from TBT



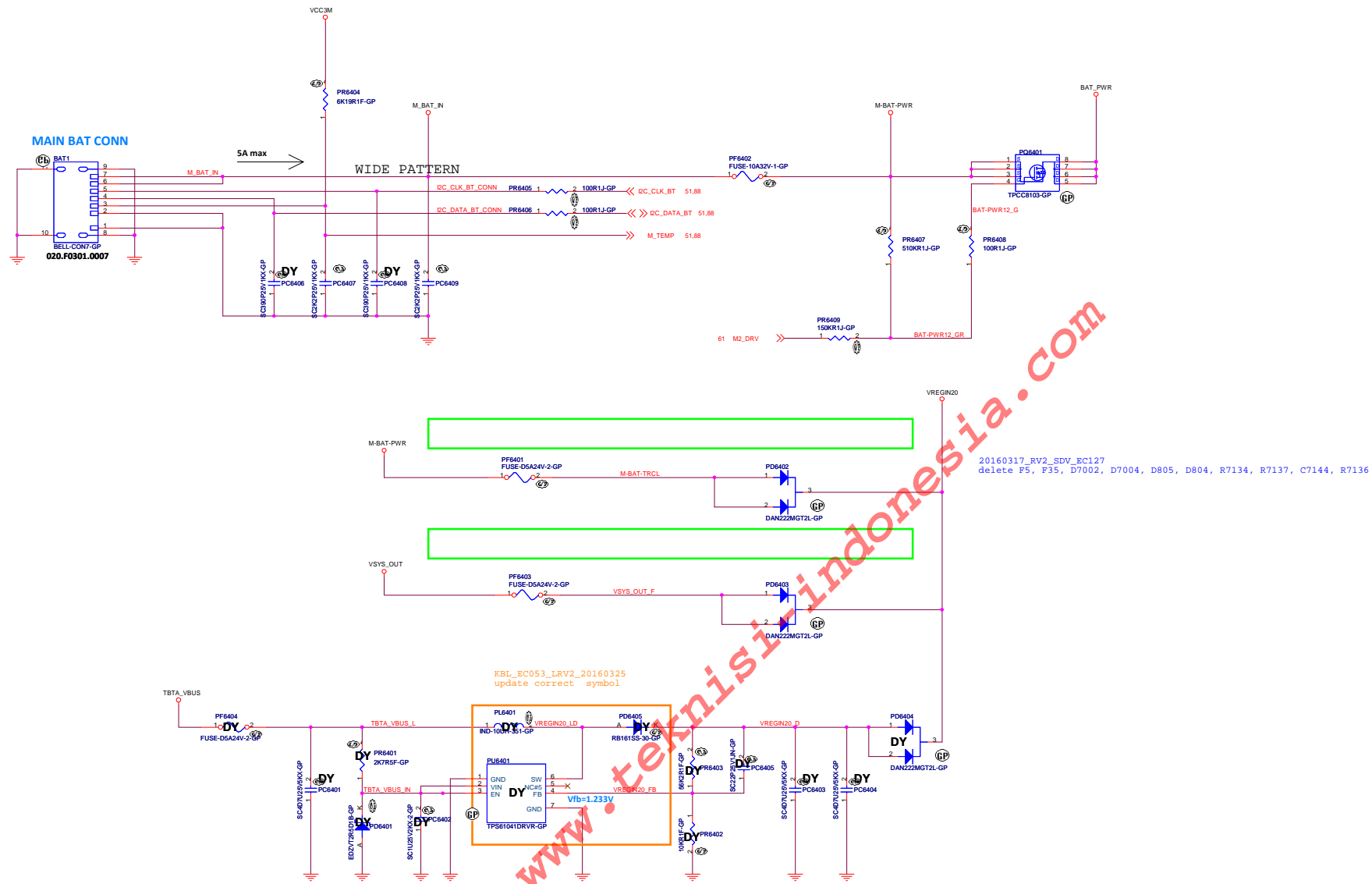
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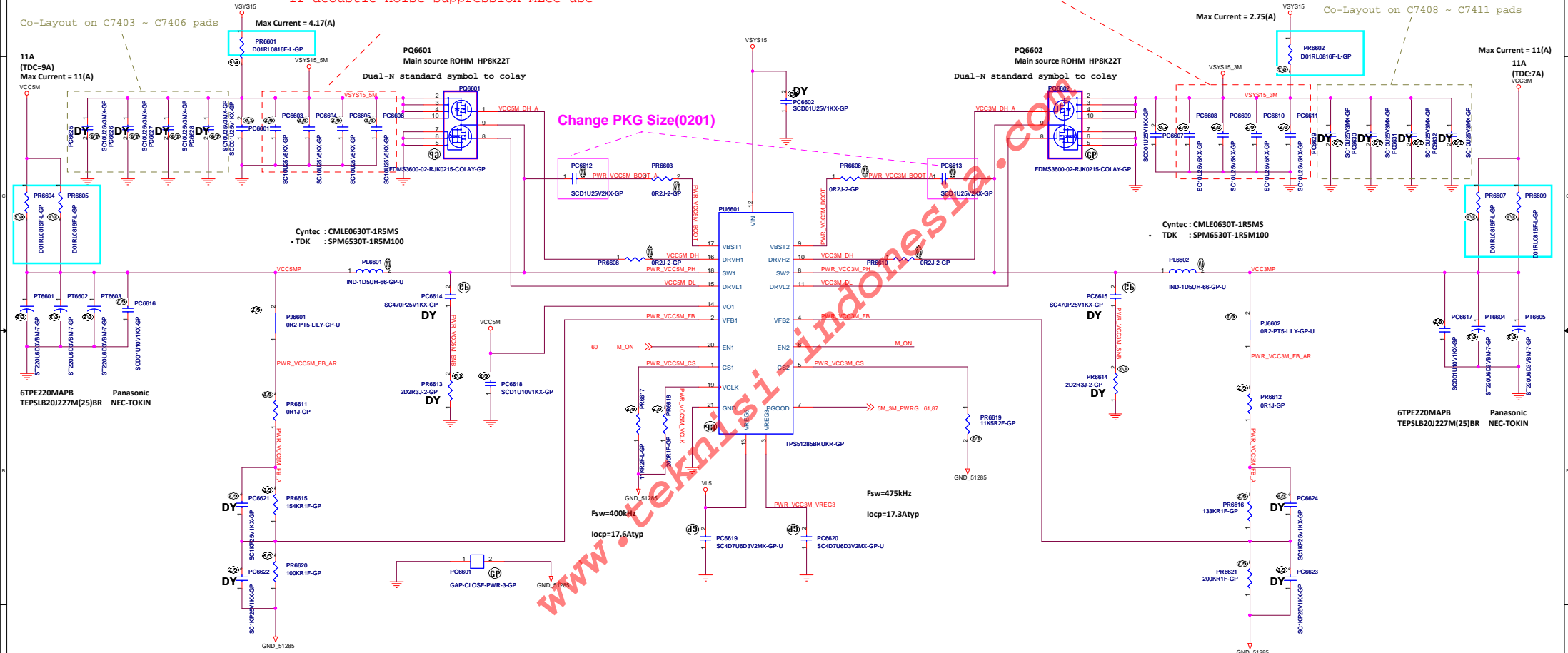
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Title BLANK	
Size A4	<div>Document Number</div> <div>Raven-2</div>
Date: Wednesday, April 27, 2016	<div>Rev</div> <div>SA</div>
Date: Wednesday, April 27, 2016	
Sheet 63 of 89	



20160406_RV2_SDV_EC162
change Cu short-pad to sense resistors
R5802, PR6601, PR6602, PR6604,
PR6605, PR6607, PR6609, PR7202, PR7304, PR7302

keep more than 2.0mm height for
if acoustic noise suppression MLCC use

keep more than 2.0mm height for
if acoustic noise suppression MLCC use



Co-Layout on C7602 ~ C7607 pads



Size A3	Document Number Raven-2	Rev SA
Date: Thursday, May 05, 2016	Sheet 68 of 89	

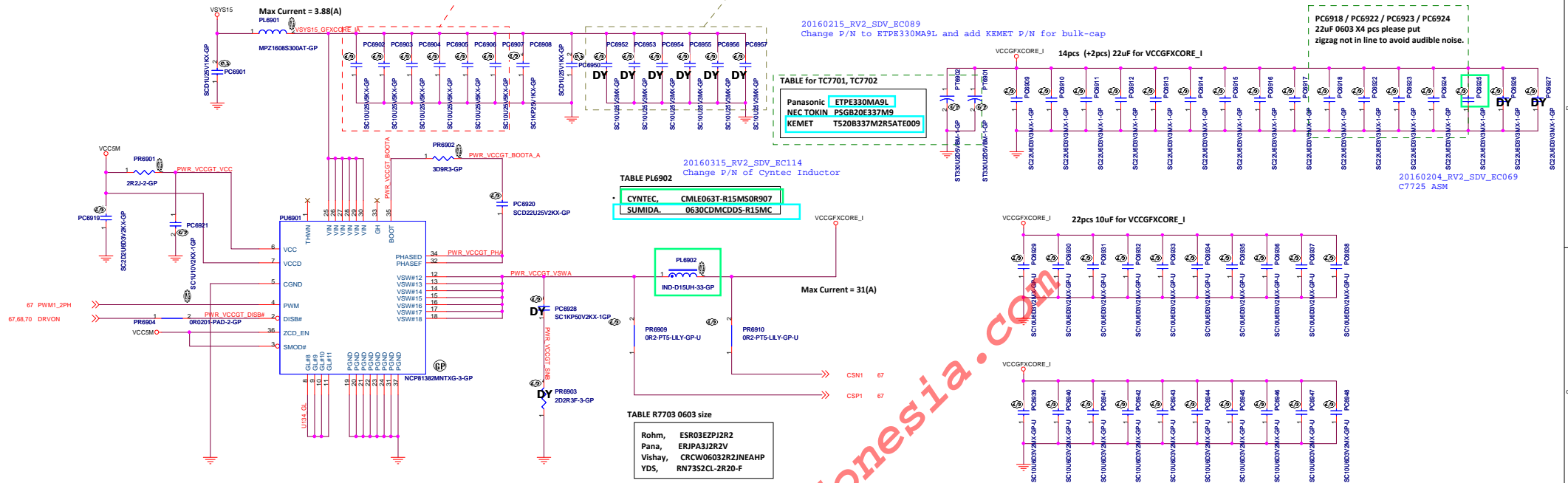
keep more than 2.0mm height for
if acoustic noise suppression MLCC use

Co-Layout on PC6952 ~ PC6957 pads

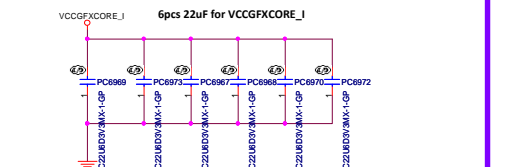
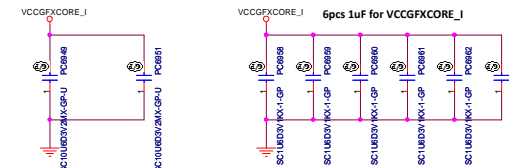
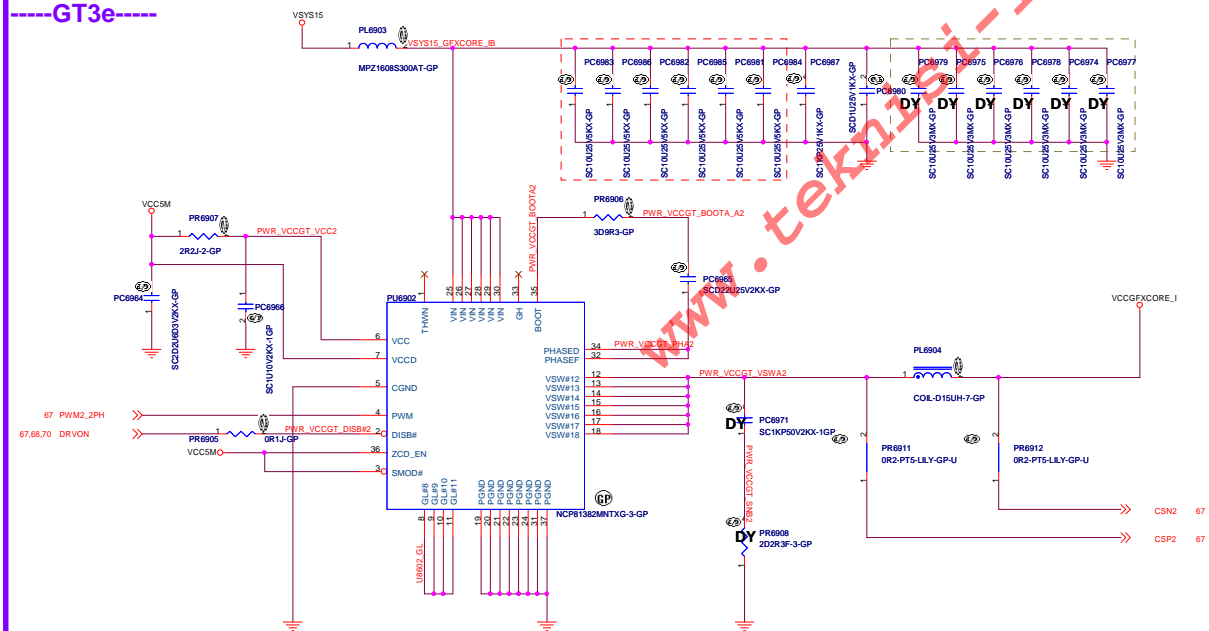
20160215_RV2_SDV_EC089

Change P/N to ETPE330MA9L and add KEMET P/N for bulk-cap

PC6918 / PC6922 / PC6923 / PC6924
22uF 0603 X4 pcs please put
zigzag not in line to avoid audible noise.

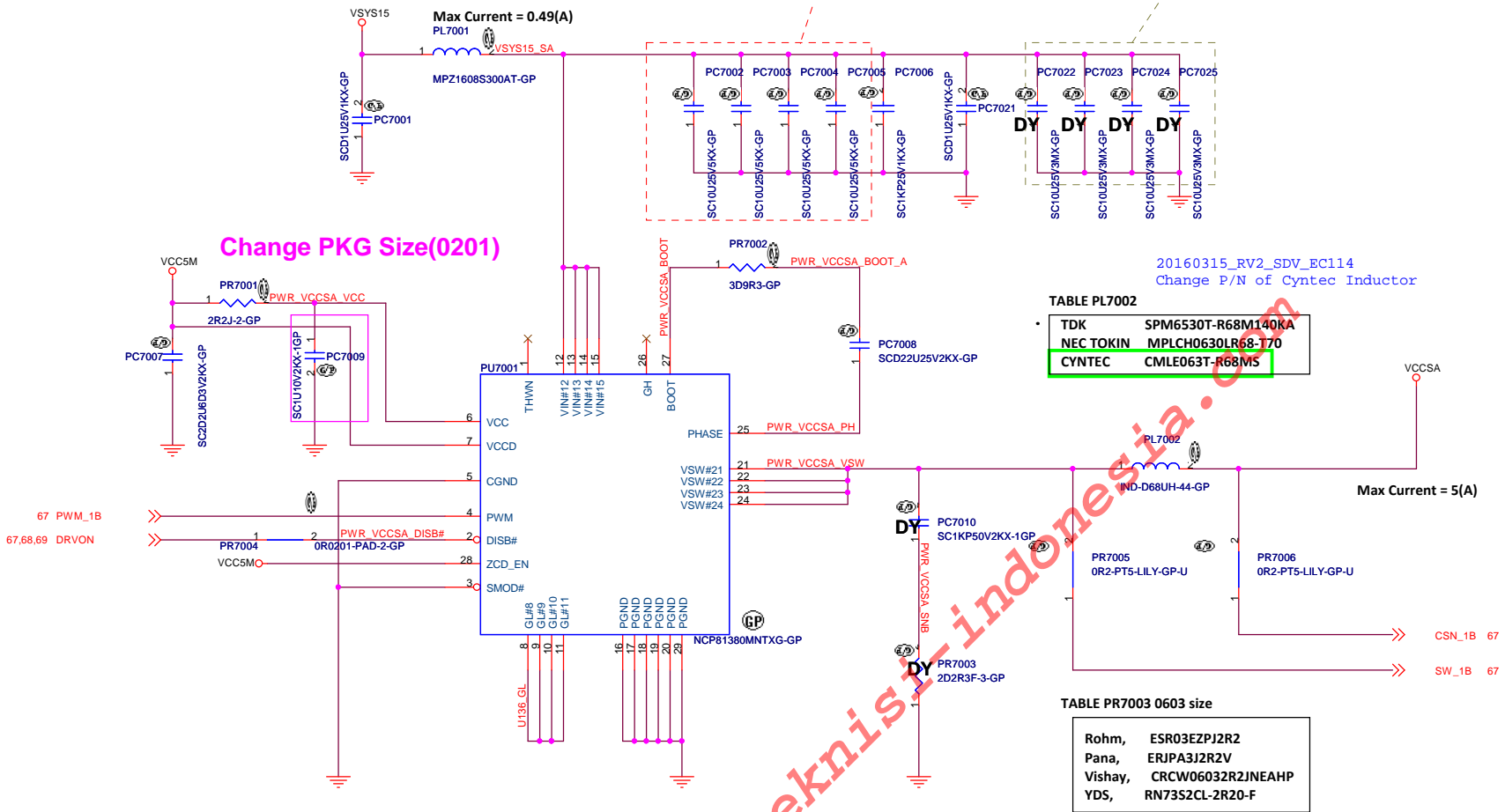


Add New Circuit
-----GT3e-----

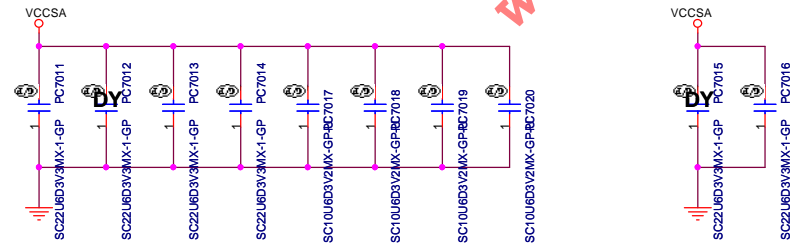


keep more than 2.0mm height for
if acoustic noise suppression MLCC use

Co-Layout on PC7022 ~ PC7025 pads



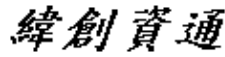
4pcs (+2pcs) 22uF and 4pcs 10uF for VCCSA



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Size A4	Document Number Raven-2		Rev SA
Date: Wednesday, April 27, 2016		Sheet 71 of	89

Change Circuit

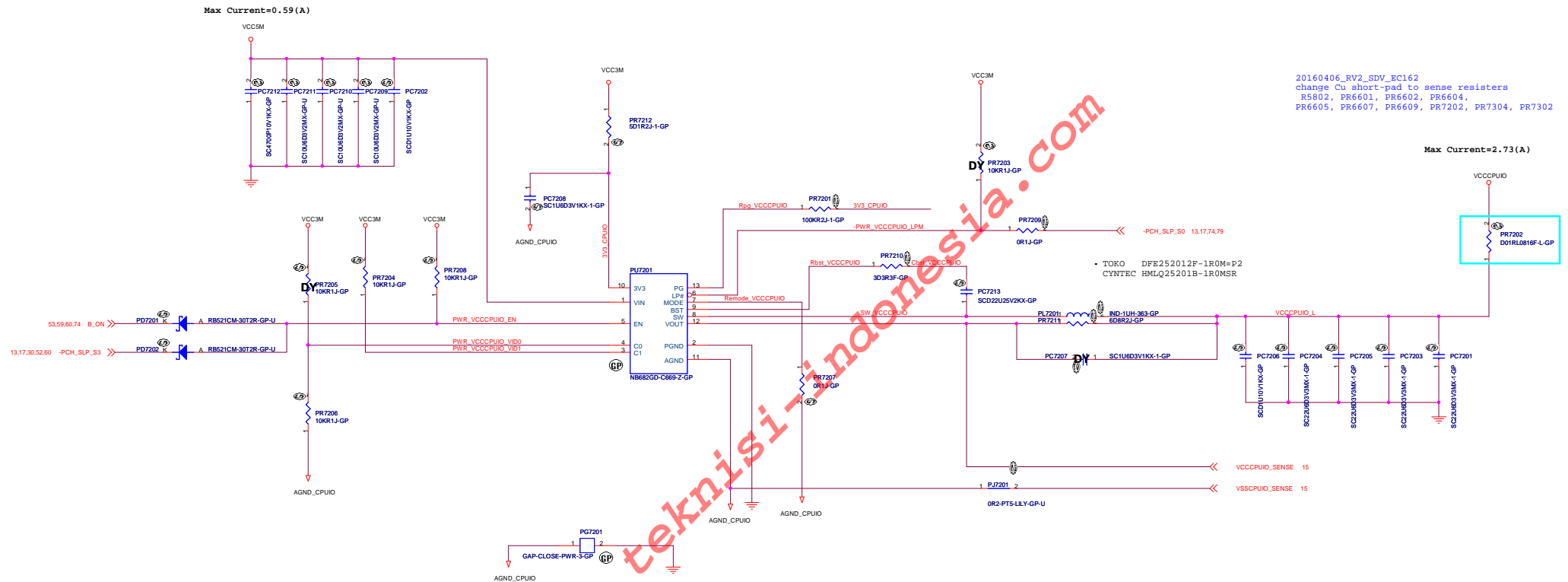
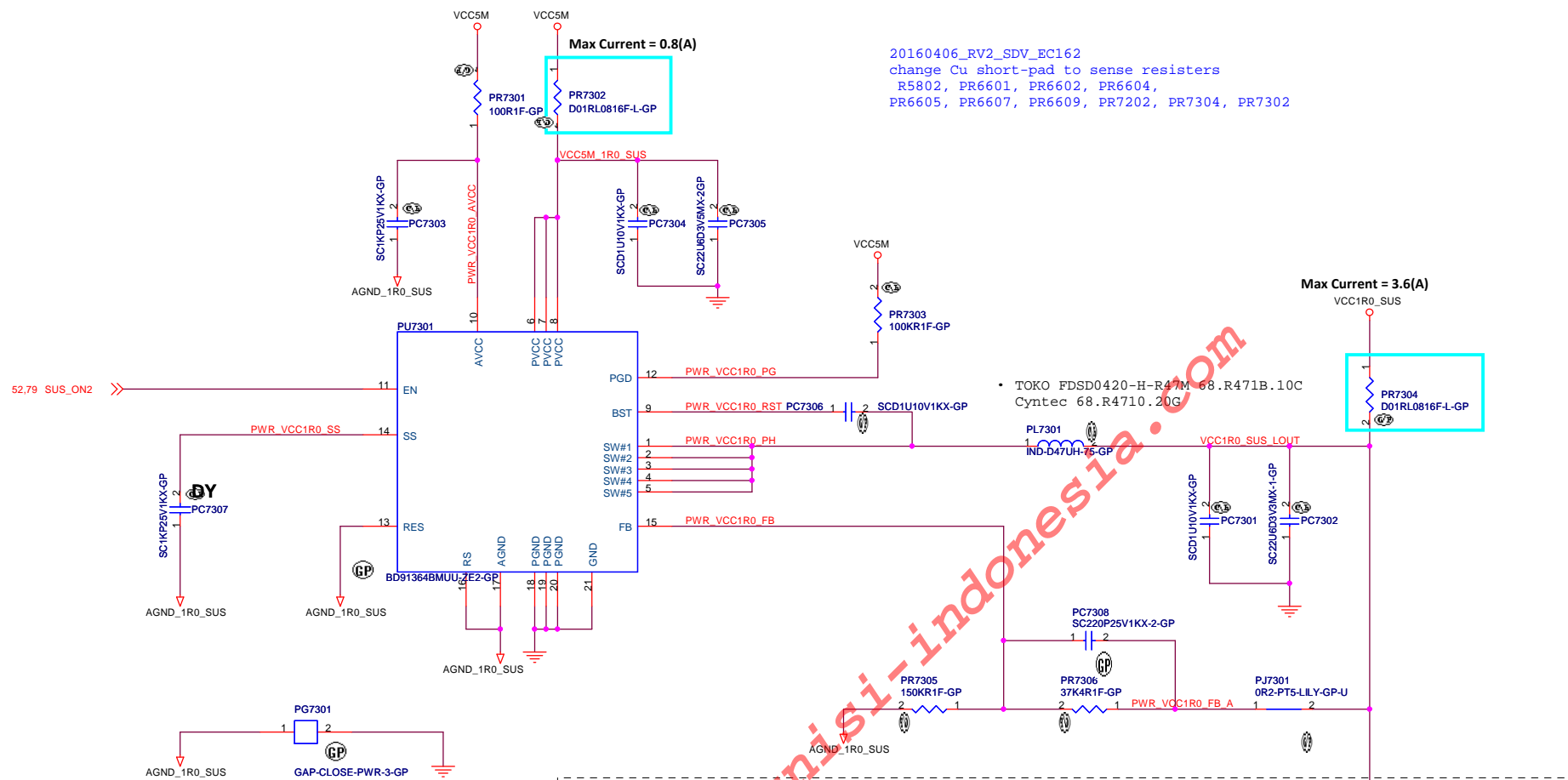


TABLE : NB682 MODE M1 (0 to GND)

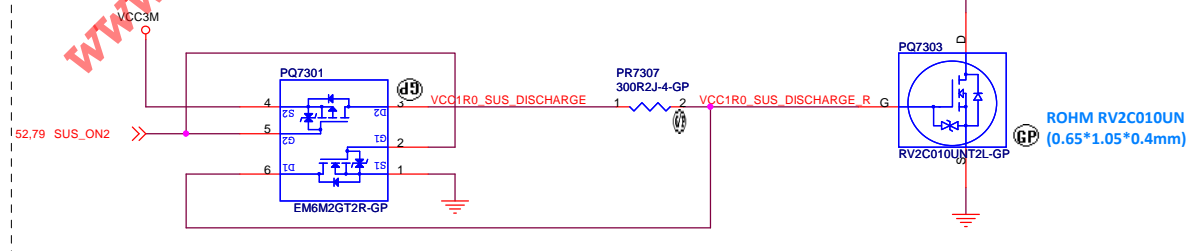
LP#	C1	C0	VOUT
0	X	X	0.000V
1	0	0	0.850V
1	0	1	0.875V
1	1	0	0.950V
1	1	1	0.975V

← SLP_S0#

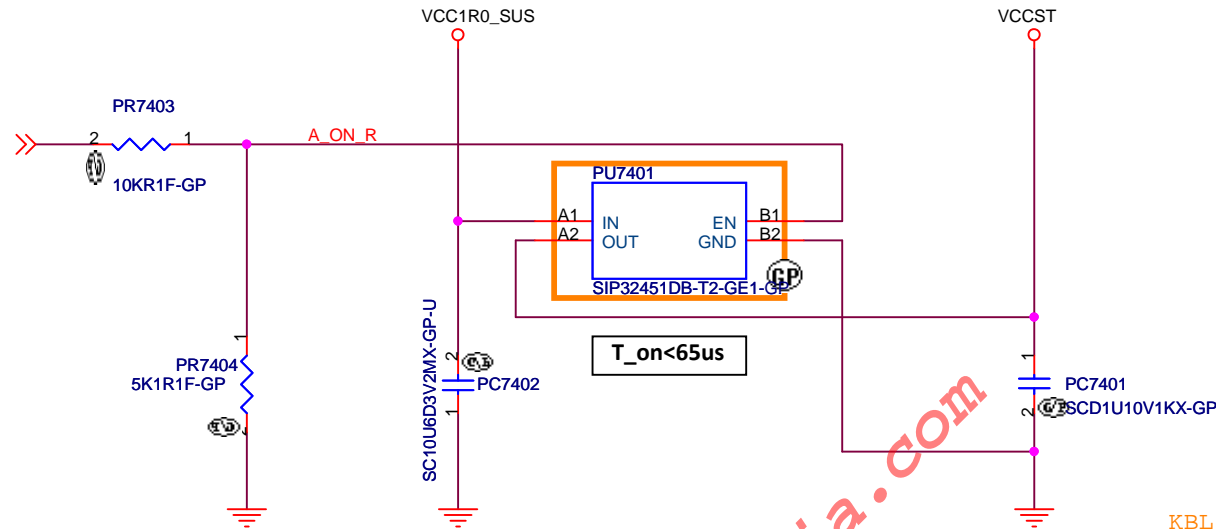
← LOGIC



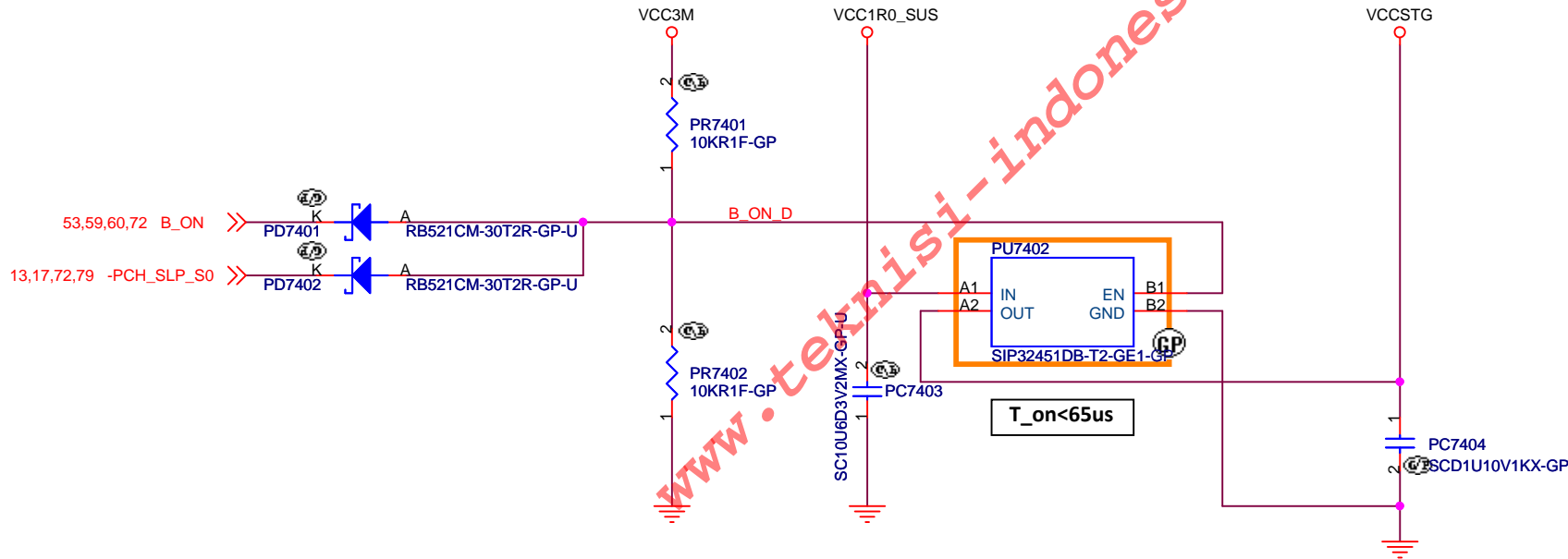
Discharge Circuit for VCC1R0_SUS
 PQ7301:ROHM EM6M2 (1.6*1.6*0.5mm) 075.00622.007C
 PQ7303:ROHM RV2C010UN (0.65*1.05*0.4mm) 084.2C010.0033
 PR7308:ROHM ESR03EZPJ2R0 (2ohm 1/4W 5% 0603) 063.2R232.015V



60,75,77 A_ON



KBL_EC045_LRV2_20160325
update correct symbol



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Title **LOAD SW VCCST & VCCSTG**

Size A4	Document Number Raven-2	Rev SA
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Date: Thursday, May 05, 2016 Sheet 74 of 89

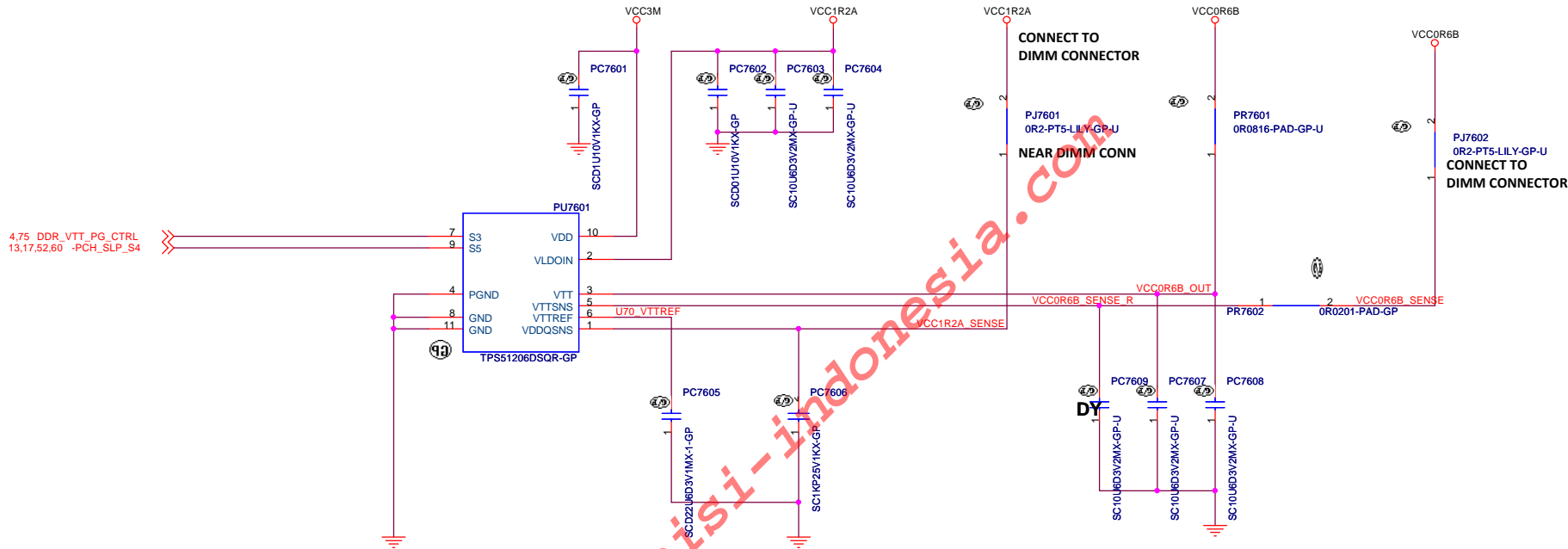
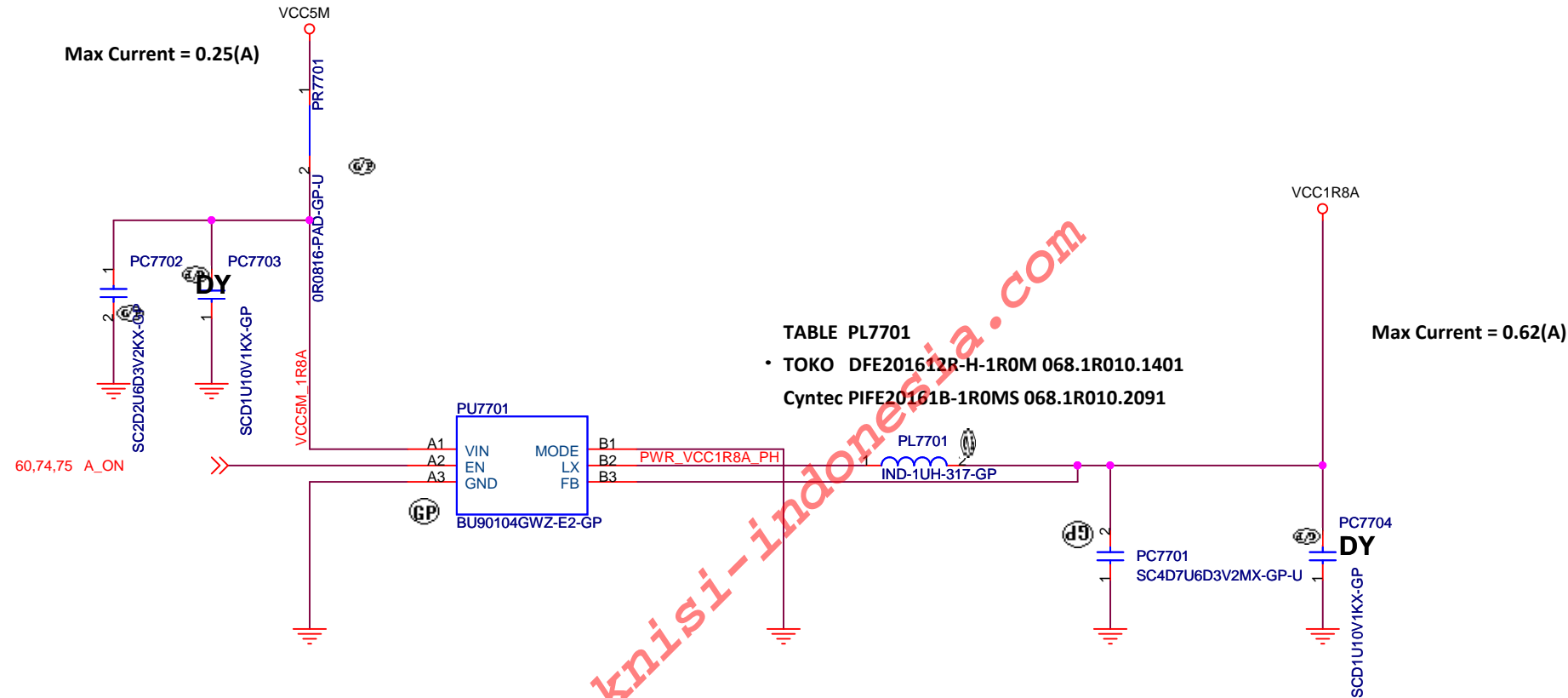


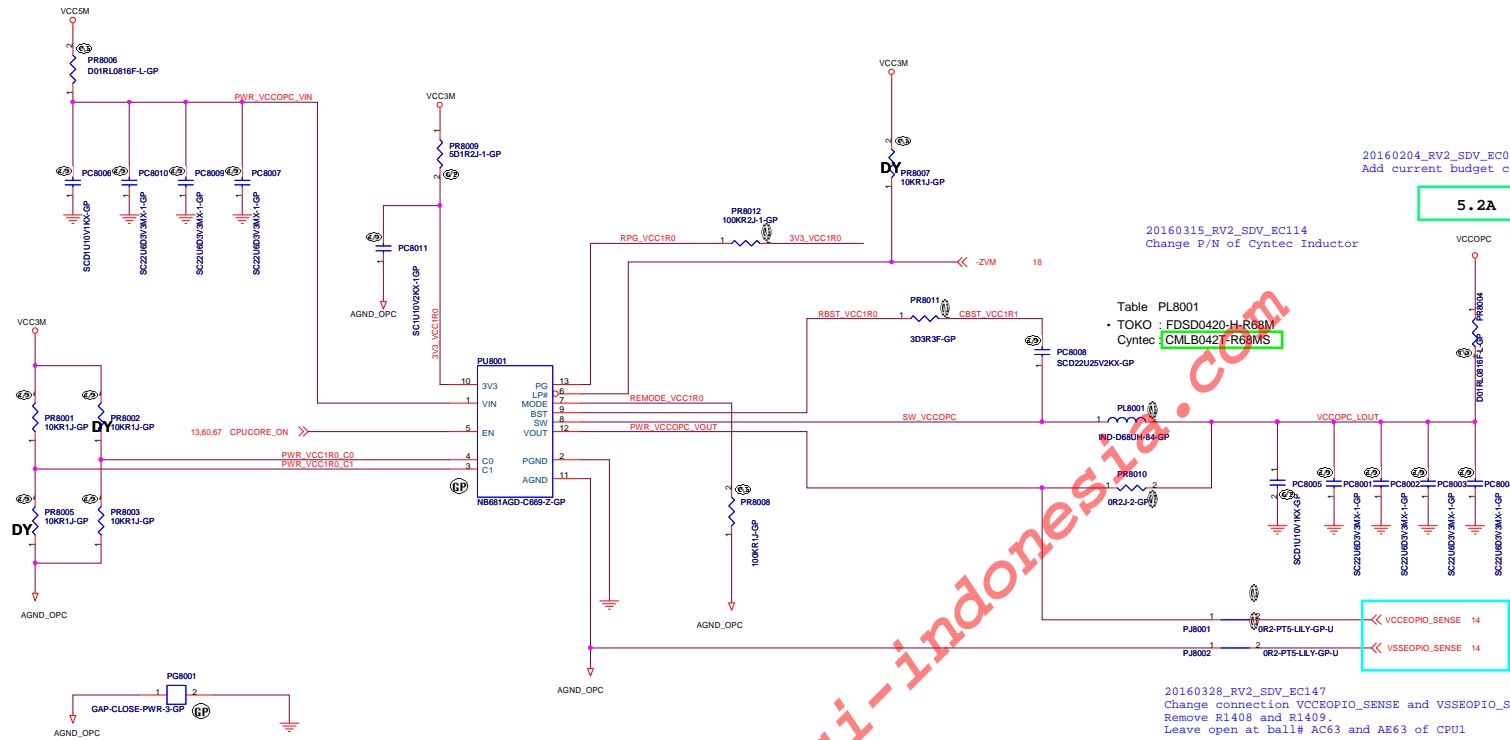
TABLE: TPS51206

S3	S5	VTT	VTTREF
High	High	ON	ON
Low	High	OFF(High-Z)	ON
Low	Low	OFF(Discharge)	OFF(Discharge)

ULT



Add New Circuit
---GT3E---



20160204_RV2_SDV_EC070
Add current budget comment for VCCOPC.

5.2A

20160315_RV2_SDV_EC114
Change P/N of Cytotec Inductor

Table PL8001
• TOKO : FDS0420-H-R68M
Cytotec : CMLB042T-R68MS

20160328_RV2_SDV_EC147
Change connection VCCOPIO_SENSE and VSSEOPIO_SENSE.
Remove R1408 and R1409.
Leave open at ball# AC63 and AE63 of CPU1

TABLE : NB681 MODE M3 (100K to GND)

LP#	C1	C0	VOUT
0	X	X	0.000V
1	0	0	0.800V
1	0	1	0.950V
1	1	0	1.000V
1	1	1	1.050V

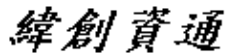
← ZVM#

← LOGIC

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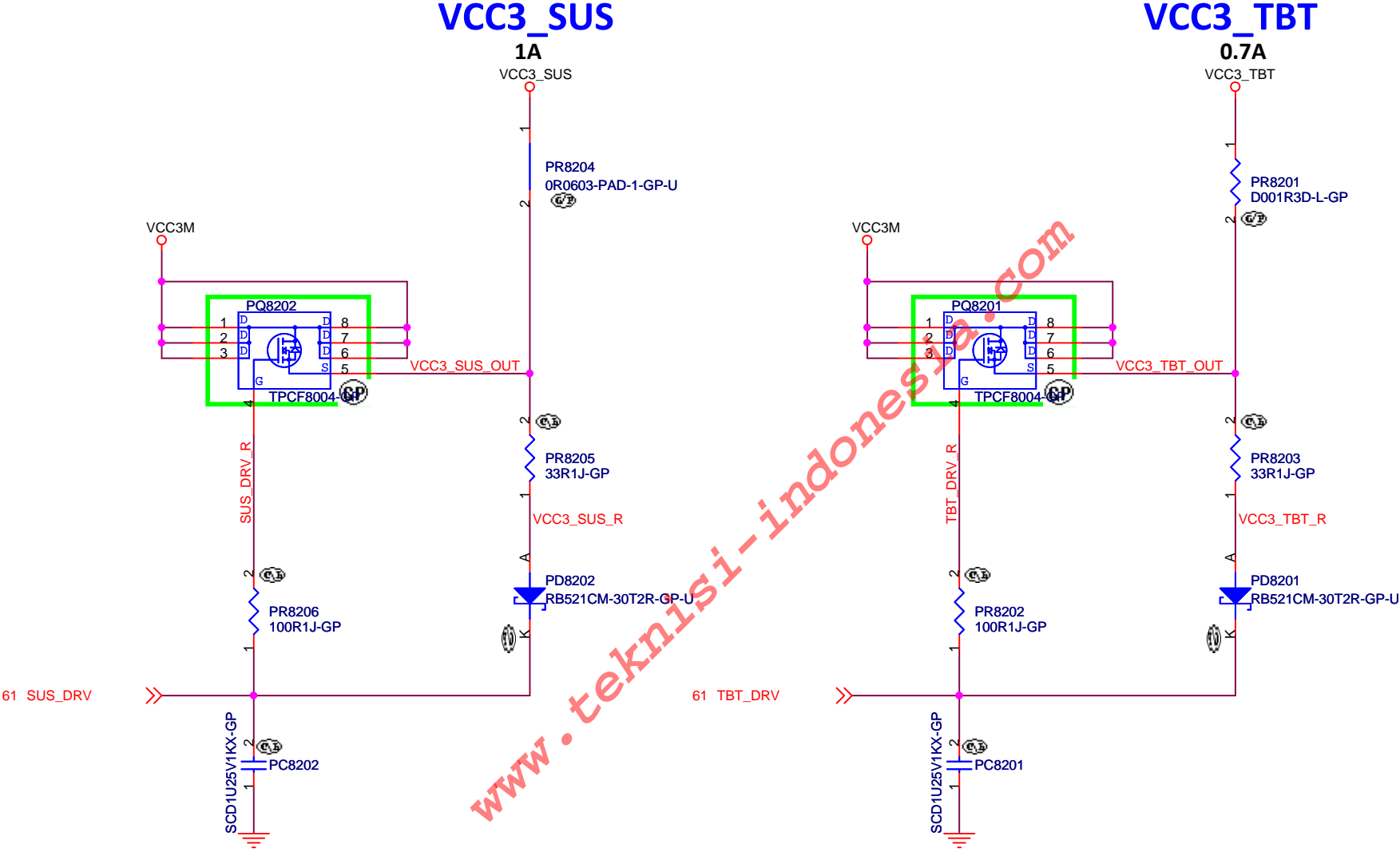
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Title BLANK			
Size A4	Document Number Raven-2		Rev SA
Date: Wednesday, April 27, 2016		Sheet 81 of	89

20160301_RV2_SDV_EC092
Change PQ8201 and PQ8202 to TPCF8004, PQ8201 and PQ8403 to RW1E014SN.

20160204_RV2_SDV_EC064
Add power SW (FET) for VCC3_TBT on VCC3M



VCC3LAN

0.5A

VCC3LAN

PR8301
0R0603-PAD-1-GP-U

VCC3LAN OUT

PR8302
33R1J-GP

VCC3LAN_R

PD8301
RB521CM-30T2R-GP-U

61 VCC3LAN_DRV >>

SCD1U25V2KX-GP

PC8301

Change PKG Size(0201)

HDMI

0.5A

VCC1R2B_HDMI

PR8304 DY D01RL0816F-L-GP

PQ8302
TPCF8004-GP

PR8305
270R1J-GP

VCC1R2B HDMI R

PD8302
RB521CM-30T2R-GP-U

61,84 VCC3B_DRV >>

SCD1U25V2KX-GP

PC8303

Change PKG Size(0201)

DY

PC8302
SCD1U10V1KX-GP

Place PC8302 near MOSFET

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Title **LOAD SW LAN/HDMI**

Size
A4

Document Number

Raven-2

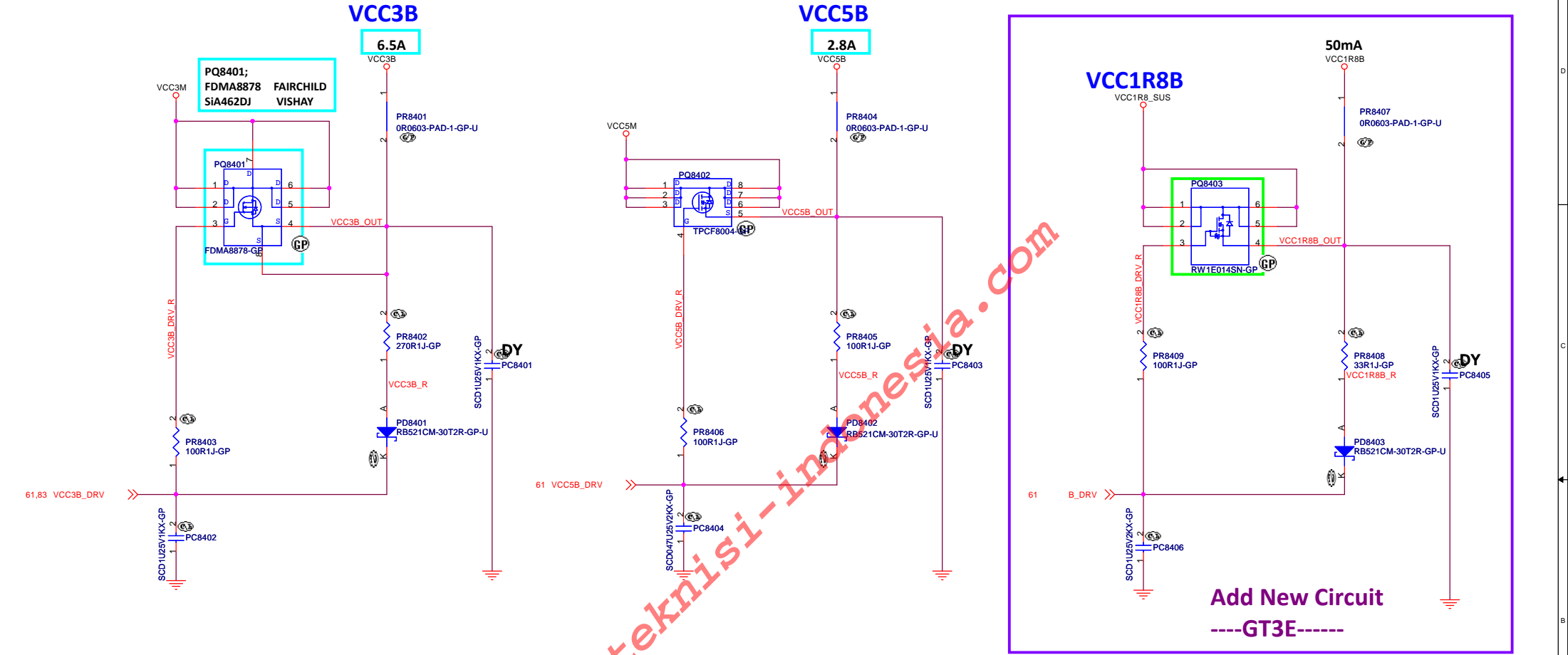
Rev
SA

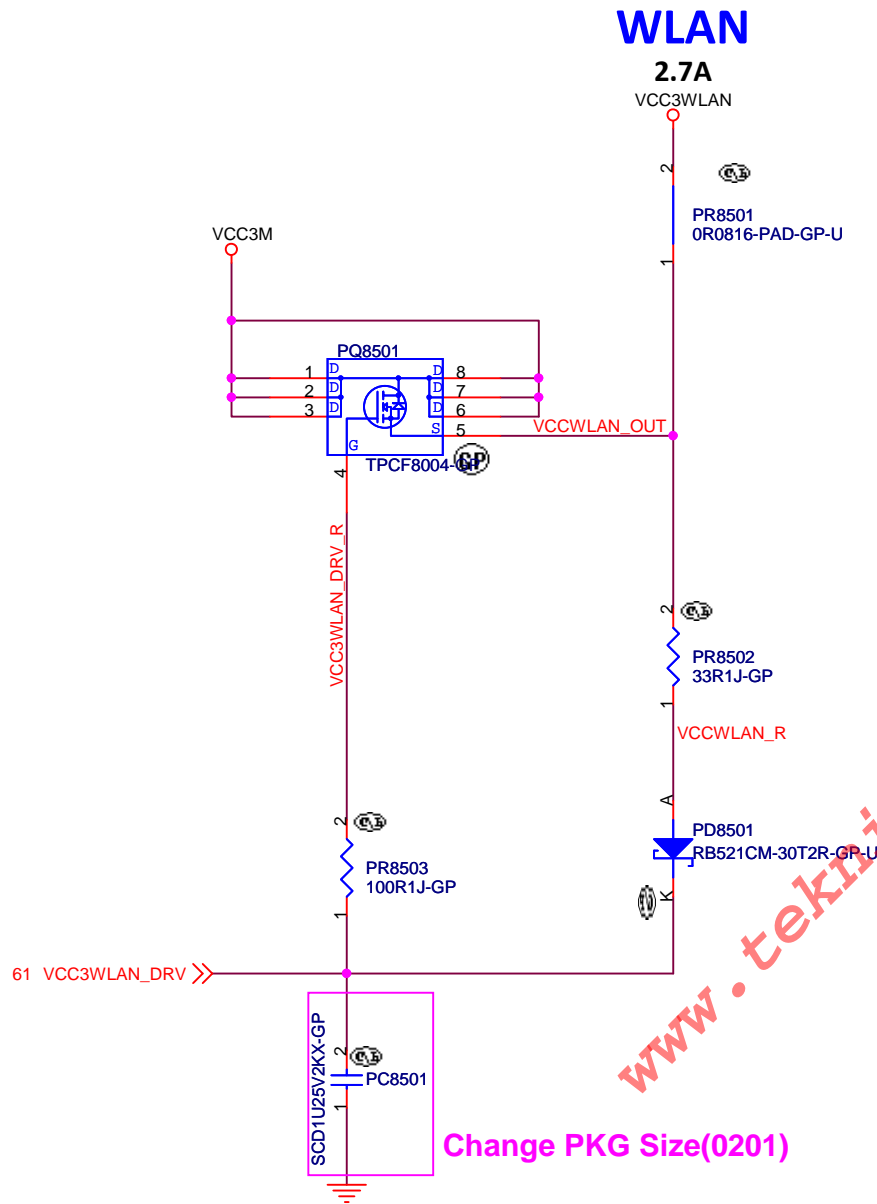
Date: Thursday, May 05, 2016

Sheet 83 of 89

20160215_RV2_SDV_EC090
Change QPQ8401 to FDMA8878 for VCC3B Load Sw
Modify current budget for VCC3B, VCC5B and VCC3_SUS.

20160301_RV2_SDV_EC092
Change PQ8402 to TPCF8004, PQ8403 to RW1E014SN.





WWAN

Delete Load SW

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Title **LOAD_SW WLAN**

Size
A4

Document Number

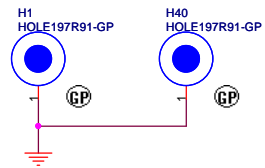
Raven-2

Rev
SA

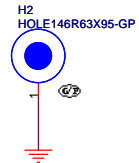
Date: Thursday, May 05, 2016

Sheet 85 of 89

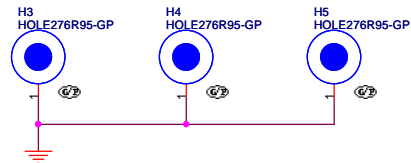
ZZ.00PAD.I81



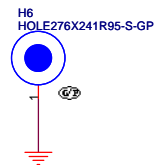
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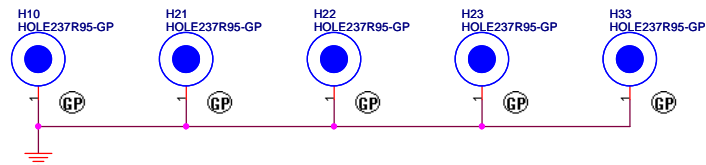
ZZ.SCREW.701



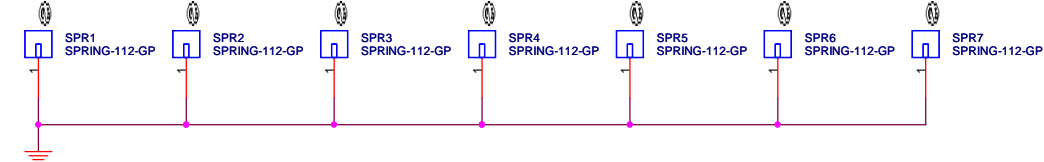
ZZ.00PAD.DK1



ZZ.00PAD.921



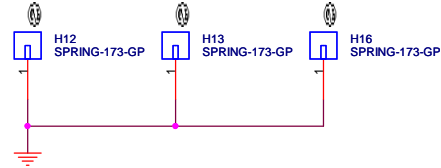
34.44401.001



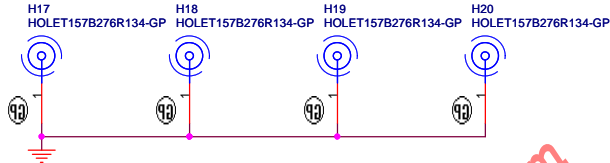
TABLE

	Yoga	Clamshell
SPR1 ~ SPR7	ASM	NO ASM

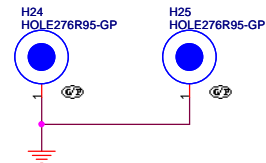
434.04P09.0001



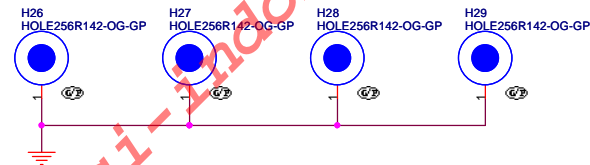
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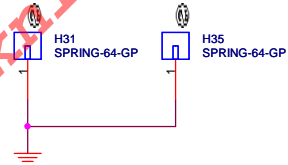
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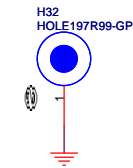
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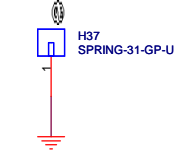
34.4H602.001



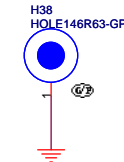
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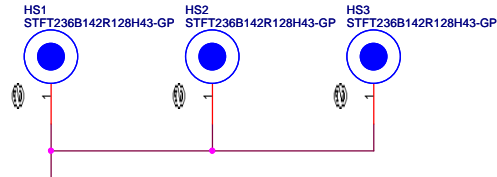
34.49U24.001



ZZ.SCREW.G91



34.4LY01.001



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Title **PTH FOR SCREW HOLES**

Size A3 Document Number **Raven-2** Rev **SA**

Date: Wednesday, April 27, 2016 Sheet 86 of 89

For Power Switch

Top side



Bottom side



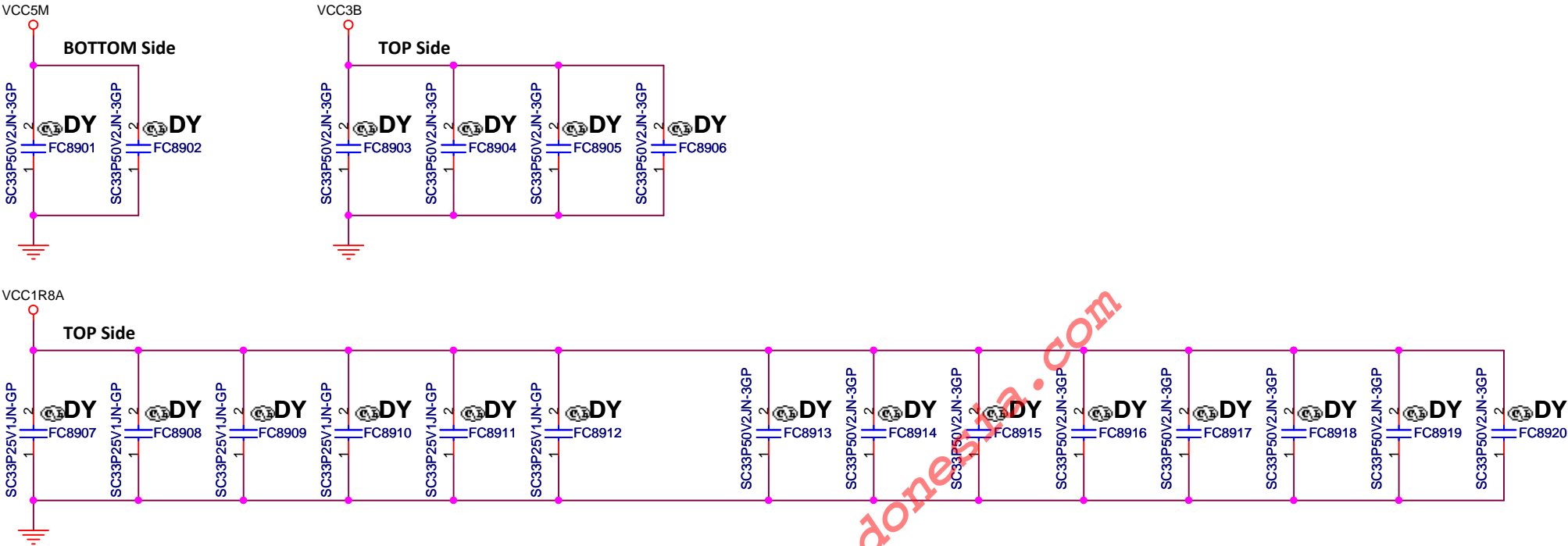
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Title EMI DECOUPLING

Size A4	Document Number Raven-2	Rev SA
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Date: Thursday, May 05, 2016 Sheet 88 of 89



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Title <div>RF</div>	
Size <div>A4</div>	Document Number <div>Raven-2</div>
Date <div>Wednesday, April 27, 2016</div>	Rev <div>SA</div>
Sheet 89 of 89	